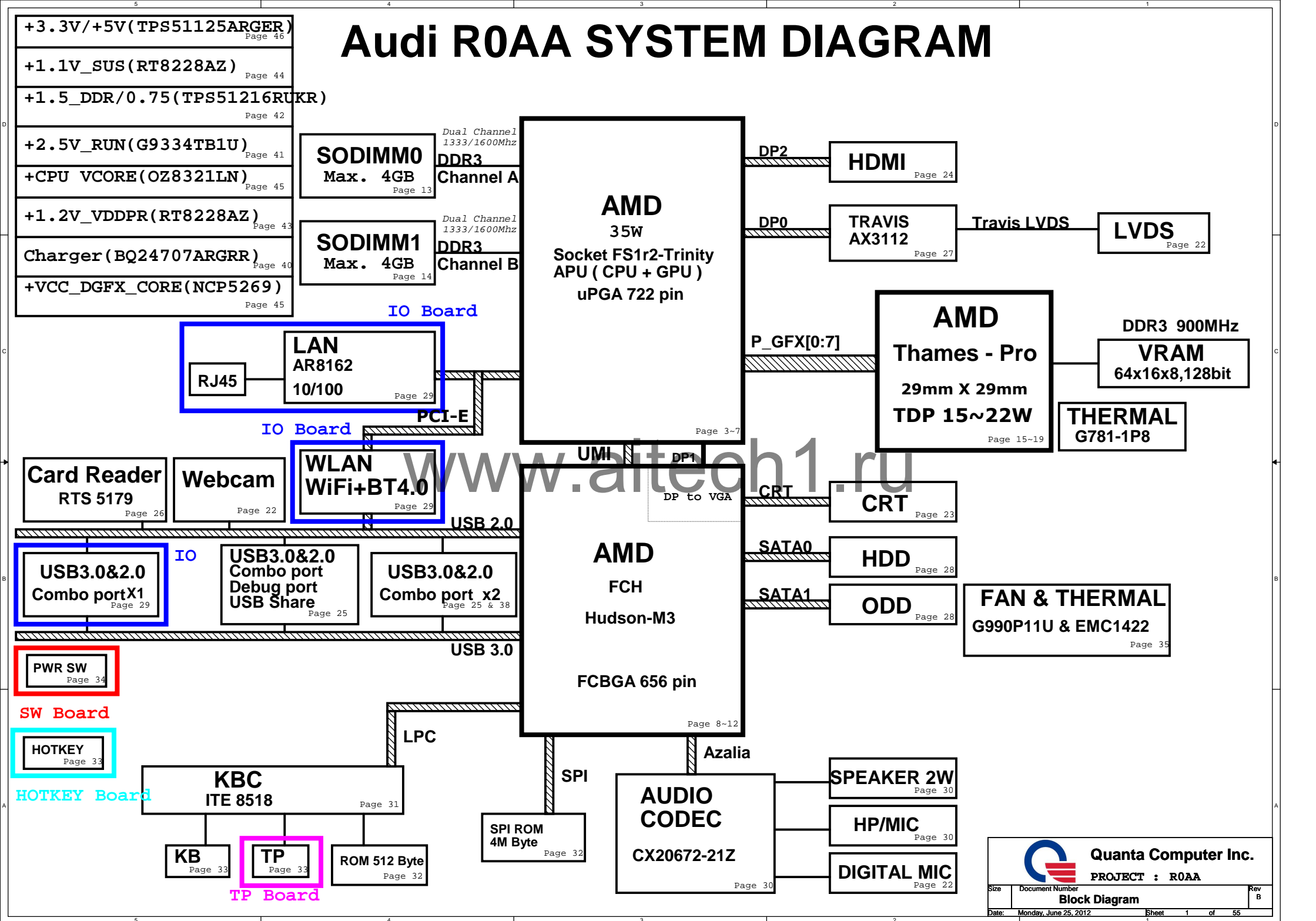


# Audi ROAA SYSTEM DIAGRAM



USB Master	Port Assignment
USB0	DEBUG
USB1	MiniCard 1 (WLAN/BT)
USB2	NC
USB3	NC
USB4	NC
USB5	NC
USB6	NC
USB7	Card Reader
USB8	NC
USB9	Camera
USB10	External port#1 (USB3.0)
USB11	External port#2 (USB3.0)
USB12	External port#3 (USB3.0)
USB13	External port#4 (Power share)

SATA Master	Port Assignment
SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

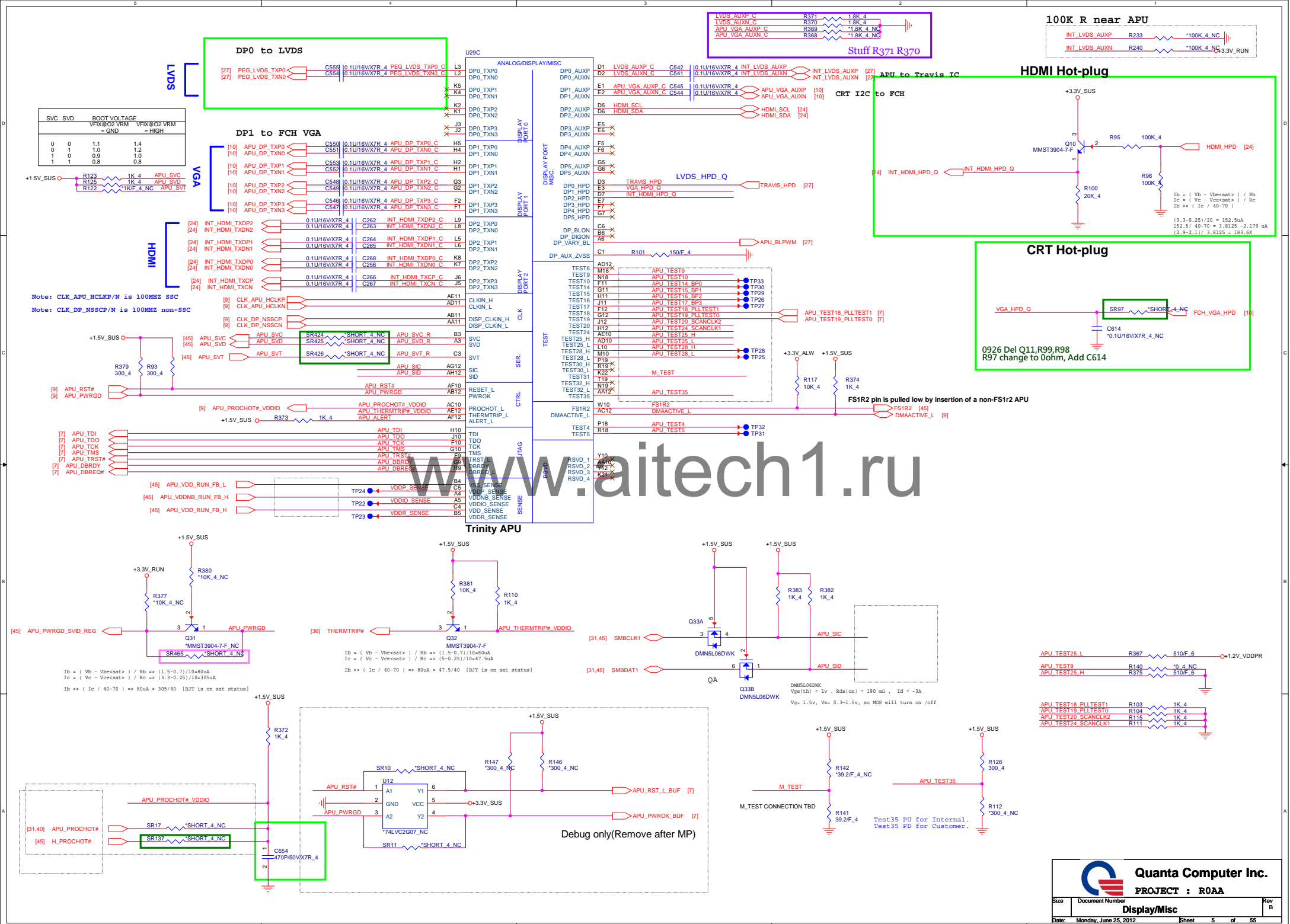
PCIE Master	Port Assignment
CPU_GPP 0	LAN
CPU_GPP 1	WLAN
CPU_GPP 2	NC
CPU_GPP 3	NC
FCH_GPP 0	NC
FCH_GPP 1	NC
FCH_GPP 2	NC
FCH_GPP 3	NC

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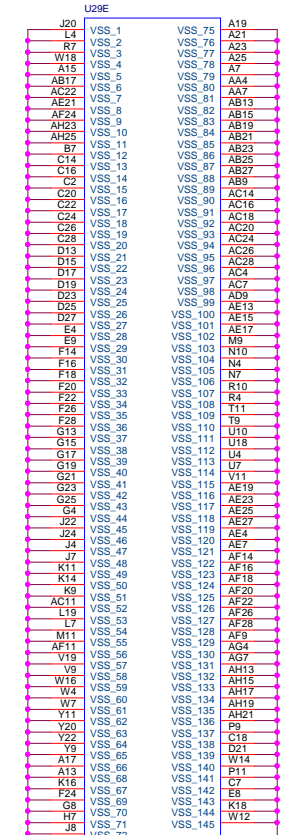
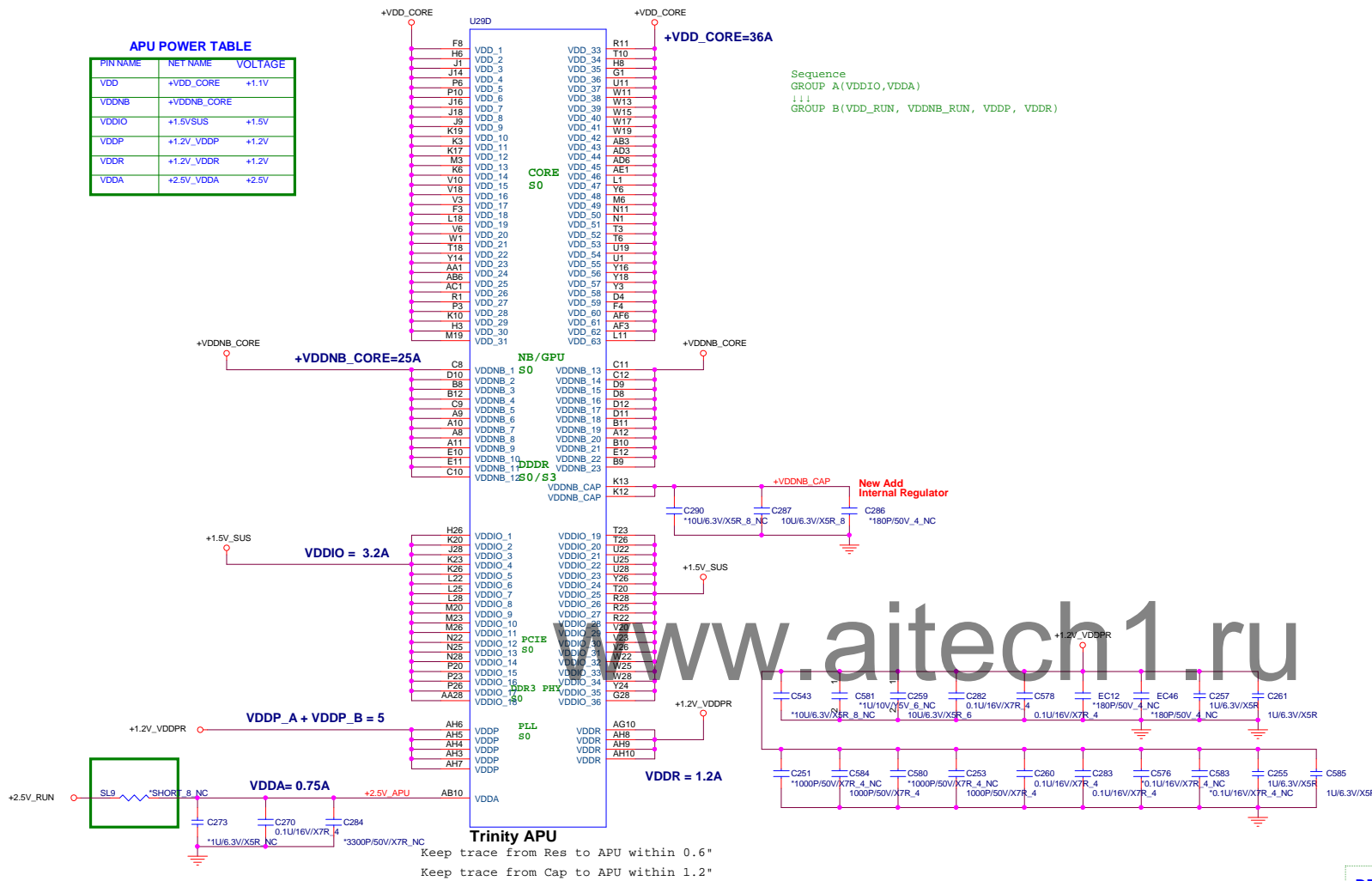






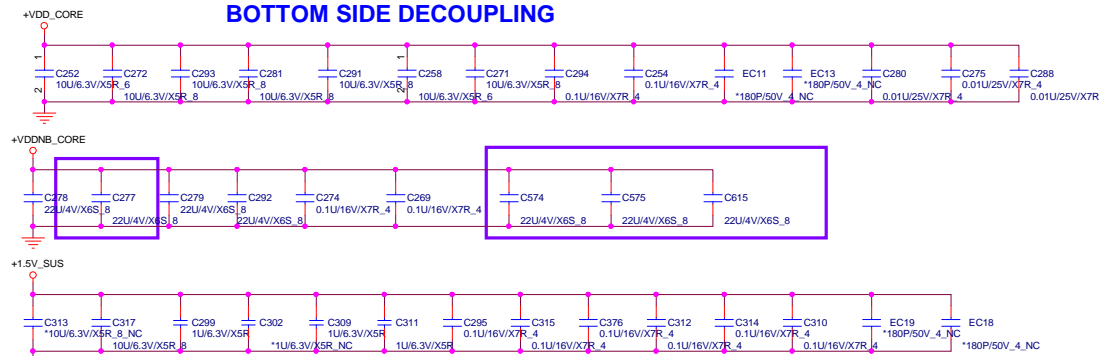


APU POWER TABLE		
PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	+1.1V
VDDNB	+VDDNB_CORE	
VDDIO	+1.5V_SUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



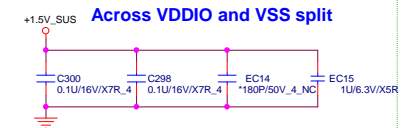
Trinity APU

## BOTTOM SIDE DECOUPLING



If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows

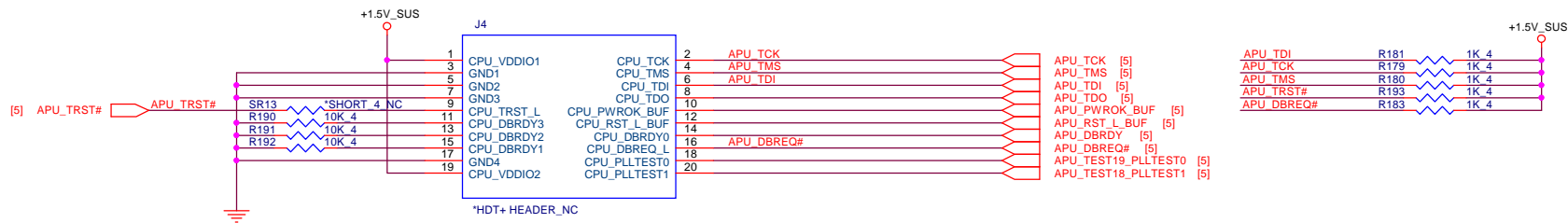
## DECOUPLING between PROCESSOR and DIMMS



Across VDDIO and VSS split

# HDT+ Connector

Debug only  
Remove after MP



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**Quanta Computer Inc.**  
**PROJECT : R0AA**

Figure 10-10: Pinmux for the APU. The diagram shows the following connections:

- MEMHOT# (TP51, TP47)
- SIO\_SLP\_S3# (SIO\_SLP\_S3#, SIO\_SLP\_S5#)
- SIO\_PWRBTN# (SIO\_PWRBTN#)
- FCH\_PWRGD (FCH\_PWRGD)
- FCH\_TEST0 (FCH\_TEST0)
- FCH\_TEST1 (FCH\_TEST1)
- FCH\_TEST2 (FCH\_TEST2)
- SIO\_A20GATE (SIO\_A20GATE)
- EC\_KBRST# (EC\_KBRST#)
- SIO\_EXT\_SC0# (SIO\_EXT\_SC0#)
- SIO\_EXT\_SM0# (SIO\_EXT\_SM0#)
- TP45 (TP45)
- TP43 (TP43)
- SIO\_EXT\_WAKE# (SIO\_EXT\_WAKE#)
- APU\_THERMTRIP# (APU\_THERMTRIP#)
- WD\_PWRGD (WD\_PWRGD)

Function	FCH port
USB12 (MB)	USB_OC0#
USB13 (MB)	*USB_OC2#
USB11 (MB)	USB_OC1#
USB10 (I/O)	USB_OC6#

3.3V\_RUN

Pin	Signal	Function
R82	2.2K 4	SMB_RUN_CLK0
R83	2.2K 4	SMB_RUN_DAT0
R22	10K 4	FCH_PCIE_WLAN_CLKREQ#
R58	10K 4	EC_KBRS1#
R218	10K 4	SIO_A20GATE
R61	10K 4	WD_PWRGD
R306	10K 4 NC	MEMHOT#
R333	10K 4 NC	SIO_EXT_SMI#
R54	10K 4	FCH_PCIE_LAN_CLKREQ#
R459	10K 4 NC	PEG_A_CLKRQ#

Timing diagram for the R276 component, showing various clock and data signals. The diagram includes signals like RSMRST#, FCH\_PCIE\_LAN\_CLKREQ#, FCH\_PCIE\_WLAN\_CLKREQ#, SMB\_RUN\_CLK0, SMB\_RUN\_DAT0, SMB\_RUN\_CLK1, SMB\_RUN\_DAT1, VGA\_PD, SPI\_HOLD#, and PEG\_A\_CLKRQ#. It also shows a TP53 test point and a SR4 component with a "SHORT CIRCUT" label. The signals are connected to various pins of the R276 component, which is a 10K 4 pin device.

Signal	Pin	Function
[29] USB_OC6#	TP46	USB OC6#
[28] SATA_ODD_PSRST#		SATA_ODD_PSRST#
[28] SATA_ODD_MD#		SATA_ODD_MD#
[16:31] AC_PRESENT		AC_PRESENT
[25] USB_OC2#		USB OC2#
[38] USB_OC1#		USB OC1#
[35] USB_OC0#		USB OC0#
		USB_OC6#/TX1/GEVENT18#
		USB_OC6#/RX0/GEVENT17#
		USB_OC4#/IR_TX0/GEVENT15#
		USB_OC3/AC_PRES/TO/GEVENT15#
		USB_OC2/TC/GEVENT14#
		USB_OC1/TDI/GEVENT13#
		USB_OC0/SPI_TPM_CS/TRST#/GEVENT12#

Timing diagram for ACZ signals. The diagram shows several digital signals over time. Signals include ACZ\_BITCLK, ACZ\_SDO, ACZ\_SDI, ACZ\_SYNC, and ACZ\_RST#. Specific points are marked with R285, R279, and R280. A large 'W' watermark is overlaid on the diagram.

```
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
PME#/GEVENT3#
LPC_SM1#/GEVENT23#
LPC_PD#/GEVENT5#
PNC_P5#/GEVENT12#
```

```
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
WD_PWRGD
```

```

RSMRST#

CLK, REQ0#/SATA, IS0#/GPIO64
CLK, REQ3#/SATA, IS1#/GPIO83
SMARTVOLT1/SATA, IS2#/GPIO50
CLK, REQ0#/SATA, IS3#/GPIO51
SATA, IS4#/FANOUT3/GPIO55
SATA, IS5#/FANOUT3/GPIO59
SPKR/GPIO66
SCLD/GPIO43
SDA0/GPIO47
SCLD/GPIO227
SDA1/GPIO228
CLK, REQ0#/FANIN4/GPIO62
CLK, REQ1#/FANOUT4/GPIO61
IR, LED2/LLB#0/SH104
SMARTVOLT2/SH104
SMARTVOLT3/SH104
DOP3, ST4/GEVENT#7#/VGA_PD
GBE, LED0/GPIO183
SPI_HOLD#/GBE, LED1/GEVENT#9
GBE, LED2/GEVENT#10
GBE, ST4/GEVENT#11
CLK, REQ0#/GPIO65/OSCIN/IDEEXIT#

```

```
BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRESDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#
```

AZ\_BITCLK  
AZ\_SDOUT  
AZ\_SDIN0.GPIO167  
AZ\_SDIN1.GPIO168  
AZ\_SDIN2.GPIO169  
AZ\_SDIN3.GPIO170  
AZ\_SYNC  
AZ\_RST#

PS2\_DAT#/SDA4#/GPIO187  
PS2\_CLK#/CEC/SC/L4#/GPIO188  
SPI\_CS2#/GBE\_STAT2#/GPIO166

PS2KB\_DAT#/GPIO189  
PS2KB\_CLK#/GPIO190  
PS2M\_DAT#/GPIO191  
PS2M\_CLK#/GPIO192

KSO\_0/GPIO209  
KSO\_1/GPIO210  
KSO\_2/GPIO211  
KSO\_3/GPIO212  
KSO\_4/GPIO213  
KSO\_5/GPIO214  
KSO\_6/GPIO215  
KSO\_7/GPIO216  
KSO\_8/GPIO217

KSO\_8/GPIO217  
KSO\_9/GPIO218  
KSO\_10/GPIO219  
KSO\_11/GPIO220  
KSO\_12/GPIO221  
KSO\_13/GPIO222  
KSO\_14/XDB0/GPIO223  
KSO\_15/XDB1/GPIO224  
KSO\_16/XDB2/GPIO225  
KSO\_17/XDB3/GPIO226

HUNSON M3  
M3\_100-CK4148(218-0755042)

EVENTS

USB 1,1

USB\_FSD00N

USB\_HSD13P

USB\_HSD13N

USB\_HSD12P

USB\_HSD12N

USB\_HSD11P

USB\_HSD11N

USB\_HSD11P  
USB\_HSD11N  
  
USB\_HSD10P  
USB\_HSD10N

GPIO	USB 2.0	
	USB_HSD9P	
	USB_HSD9N	
	USB_HSD8P	
	USB_HSD8N	
	USB_HSD7P	
	USB_HSD7N	
	USB_HSD6P	
	USB_HSD6N	
	USB_HSD5P	
	USB_HSD5N	
	USB_HSD4P	
	USB_HSD4N	
	USB_HSD3P	
	USB_HSD3N	
	USB_HSD2P	
	USB_HSD2N	

USB\_OC

USB\_SS\_TX3P  
USB\_SS\_TX3N  
  
USB\_SS\_RX3P  
USB\_SS\_RX3N  
  
USB\_SS\_TX2P  
USB\_SS\_TX2N  
  
USB\_SS\_RX2P  
USB\_SS\_RX2N

USB	USB_SS_TX1P
3.0	USB_SS_TX1N
	USB_SS_RX1P
	USB_SS_RX1N
	USB_SS_TX0P
	USB_SS_TX0N
	USB_SS_RX0P
	USB_SS_RX0N

EC\_PWM0/EC\_TIMER0/GPIO197  
EC\_PWM1/EC\_TIMER1/GPIO198  
M2/EC\_TIMER2/WOL\_EN/GPIO199  
EC\_PWM2/EC\_TIMER3/GPIO200

```
EC_FWM3/EC_TIMER3/GPIO200
KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208
```

---

H10		USBP13P	[25]
G10		USBP13N	[25]
K10		USBP12P	[25]
J12		USBP12N	[25]
G12		USBP11P	[25]






F12	USBP11P	[38]
	USBP11N	[38]
K12	USBP10P	[29]
K13	USBP10N	[29]

Diagram illustrating the location of the USBP9 and USBP7N genes on the human genome. The USBP9 gene is located on chromosome 11, and the USBP7N gene is located on chromosome 7. The diagram also shows the location of other genes: USBP9P, USBP9N, USBP7P, and USBP7N. The USBP9 and USBP7N genes are shown with a red 'X' mark, indicating a deletion or mutation. The USBP9P and USBP9N genes are shown with a red 'X' mark, indicating a deletion or mutation. The USBP7P and USBP7N genes are shown with a red 'X' mark, indicating a deletion or mutation.

[illegible]

C14		USB3_TXP3	[25]
		USB3_TXN3	[25]
C12			
A12		USB3_RXP3	[24]
		USB3_RXN3	[24]
D15			
B15		USB3_TXP2	[25]
		USB3_TXN2	[25]
E14			
F14		USB3_RXP2	[24]
		USB3_RXN2	[24]

F15			USB3_TXP1	[38]
G15			USB3_TXN1	[38]
H13			USB3_RXP1	[38]
G13			USB3_RXN1	[38]
J16			USB3_TXP0	[25]
H16			USB3_TXN0	[25]
J15			USB3_RXP0	[25]

K15  USB3\_RXN0 [2]  
 H19 SMB RUN CLK2  
 G19 SMB RUN DAT2  
 G22 SMB LV CLK  
 G21 SMB LV DAT  
 E22   
 H22   
 J22   
 H21   
 EC\_PWM2 [12]

K21	X
K22	X
F22	X
F24	X
E24	X
B23	X
C24	X
F18	X

USB 3.0/2.0 Combo

USB 3.0/2.0 Combo

Camera

Card Reader

WLAN

Debug

v\_SUS

5] } USB 3.0/2.0 Combo (MB)

5] } USB 3.0/2.0 Combo (MB)

USB 3.0/2.0 Combo (MB)

USB 3.0/2.0 Combo (IO)

```

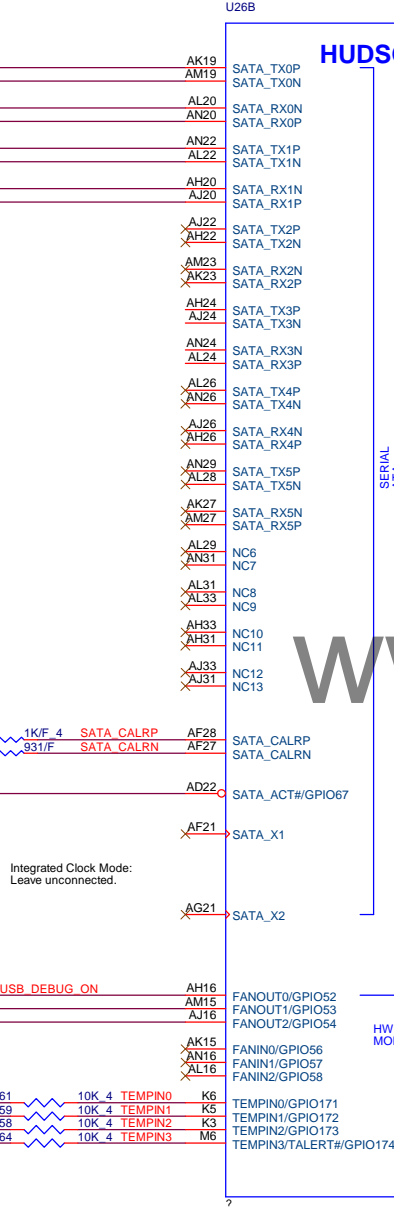
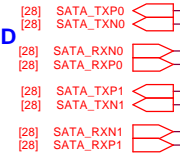
e Connector , C79~C82 stuff 0 ohm

```



SATA HDD/SSD

SATA ODD



HUDSON-M2

Part 2 of 5  
SD\_CLK/SCLK\_0/GPIO73  
SD\_CMD/SLOAD\_0/GPIO74  
SD\_CD#/GPIO75  
SD\_WP/GPIO76  
SD\_DATA0/SDAT1\_0/GPIO77  
SD\_DATA1/SDAT0\_0/GPIO78  
SD\_DATA2/GPIO79  
SD\_DATA3/GPIO80  
GBE\_COL  
GBE\_CRS  
GBE\_MDCK  
GBE\_MDIO  
GBE\_RXCLK  
GBE\_RXD3  
GBE\_RXD2  
GBE\_RXD1  
GBE\_RXD0  
GBE\_RXCTL/RXDV  
GBE\_RXERR  
GBE\_TXCLK  
GBE\_TXD3  
GBE\_TXD2  
GBE\_TXD1  
GBE\_TXD0  
GBE\_TXCTL/TXEN  
GBE\_PHY\_PD  
GBE\_PHY\_RST#  
GBE\_PHY\_INTR

SPI DI/GPIO164  
SPL\_DO/GPIO163  
SPL\_CLK/GPIO162  
SPL\_CS#/GPIO165  
ROM\_RST#/SPI\_WP#/GPIO161

VGA\_RED  
VGA\_GREEN  
VGA\_BLUE  
VGA\_HSYNCG/GP068  
VGA\_VSYNCG/GP069  
VGA\_DDC\_SDA/GP070  
VGA\_DDC\_SCL/GP071  
VGA\_DAC\_RSET  
AUX\_VGA\_CH\_P  
AUX\_VGA\_CH\_N  
AUXCAL

ML\_VGA\_L0P  
ML\_VGA\_L0N  
ML\_VGA\_L1P  
ML\_VGA\_L1N  
ML\_VGA\_L2P  
ML\_VGA\_L2N  
ML\_VGA\_L3P  
ML\_VGA\_L3N  
ML\_VGA\_HPDI/GPIO229

VIN0/GPIO175  
VIN1/GPIO176  
VIN2/SDAT1\_1/GPIO177  
VIN3/SDAT0\_1/GPIO178  
VIN4/SLOAD\_1/GPIO179  
VIN5/SCLK\_1/GPIO180  
VIN6/GBE\_STAT3/GPIO181  
VIN7/GBE\_LED3/GPIO182

FANOUT0/GPIO52  
FANOUT1/GPIO53  
FANOUT2/GPIO54  
FANIN0/GPIO56  
FANIN1/GPIO57  
FANIN2/GPIO58

TEMPIN0/GPIO171  
TEMPIN1/GPIO172  
TEMPIN2/GPIO173  
TEMPIN3/TALERT#/GPIO174

AL14  
AJ12  
AH12  
AK13  
AM13  
AH15  
AJ14

AC4  
AD3  
AD9  
W10  
AB8  
AH7  
AF7  
AE7  
AD7  
AG8  
AD1  
AF9  
AB7  
AG6  
AE8  
AD8  
AB9  
AC2  
AA7  
W9

V6  
V5  
V3  
T6  
V1

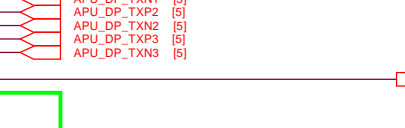
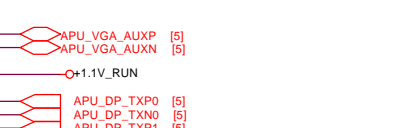
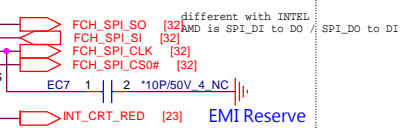
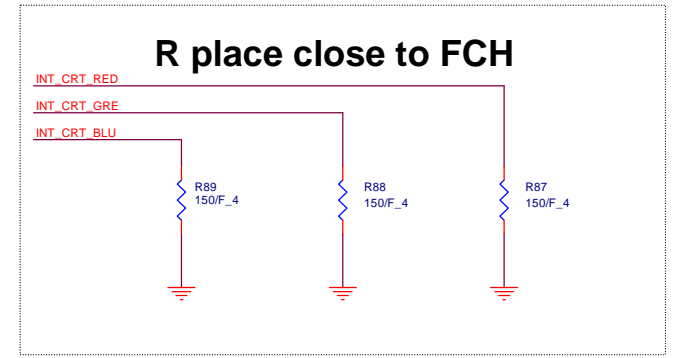
L30  
L32  
M29  
M28  
N30  
M33  
N32

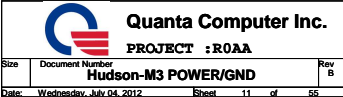
K31  
V28  
V29  
U28  
T31  
T33  
T29  
T28  
R32  
R30  
P29  
P28

C29  
N2  
M3  
L2  
N4  
P1  
P3  
M1  
M5

AG16  
AH10  
A28  
G27  
L4

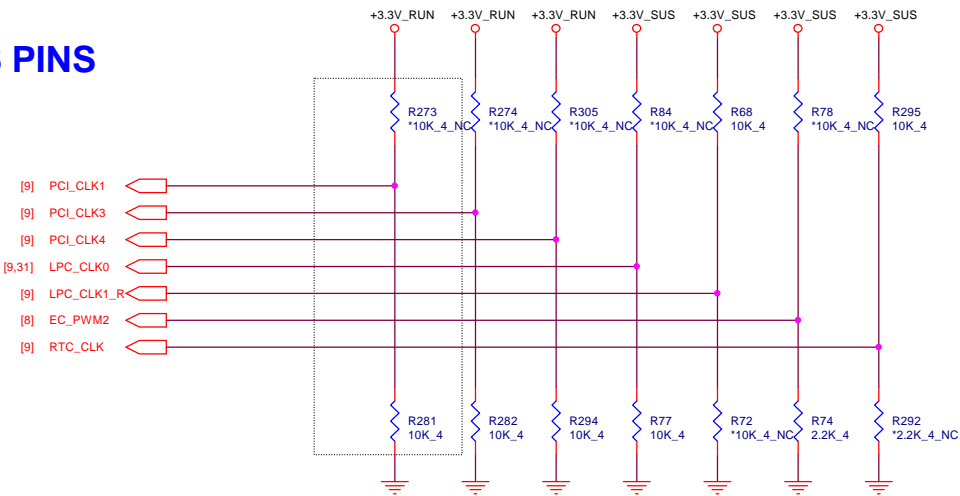
check







STRAPS PINS

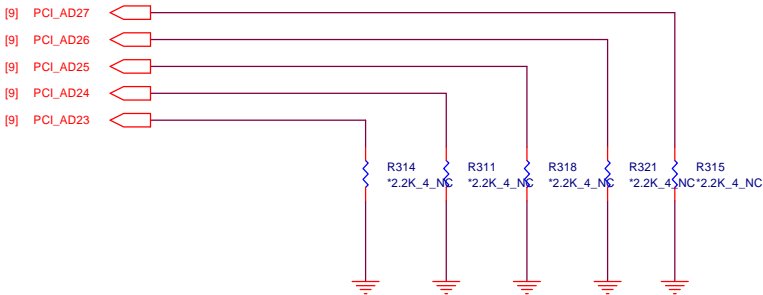


REQUIRED STRAPS

	-----	PCI_CLK1	-----	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	-----	ALLOW PCIe Gen2	-----	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED  Setting	LPC ROM	S5 PLUS MODE DISABLED  Setting
PULL LOW	-----	FORCE PCIe Gen1  Setting	-----	IGNORE DEBUG STRAP  Setting	FUSION CLOCK MODE  Setting	EC DISABLED  Setting	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE ENABLED  Setting

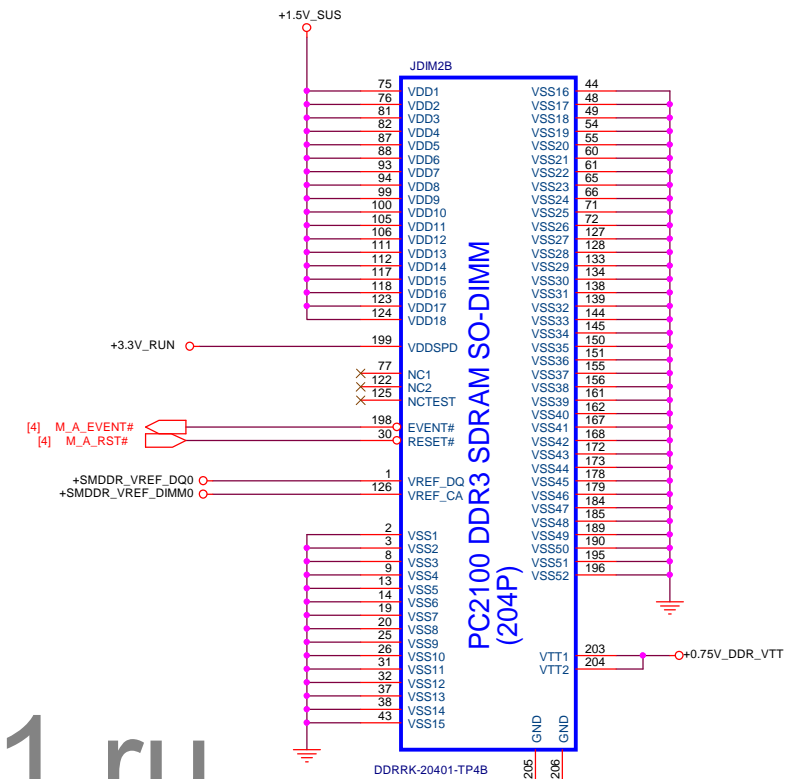
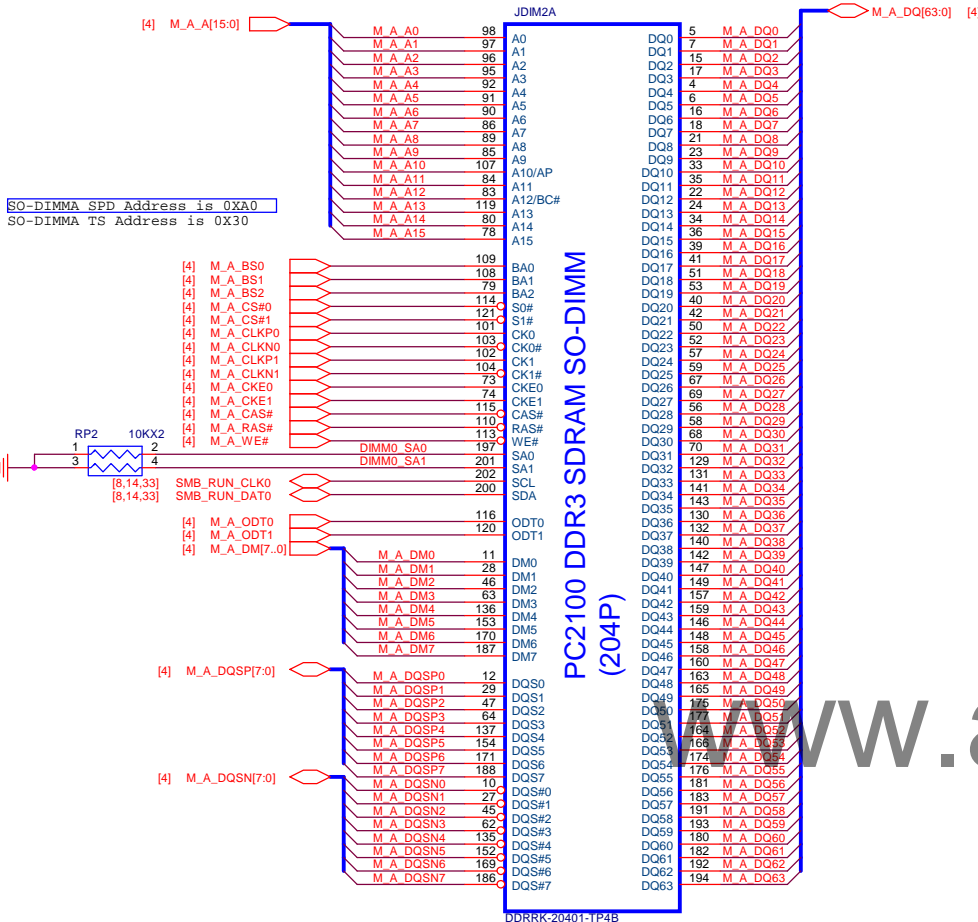
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

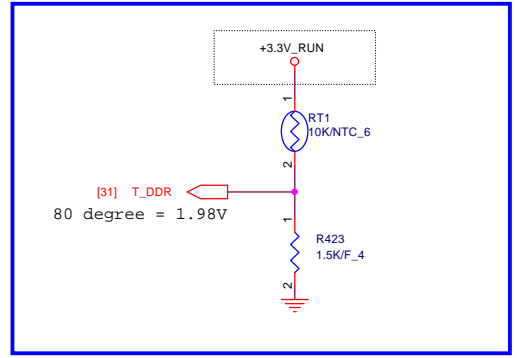
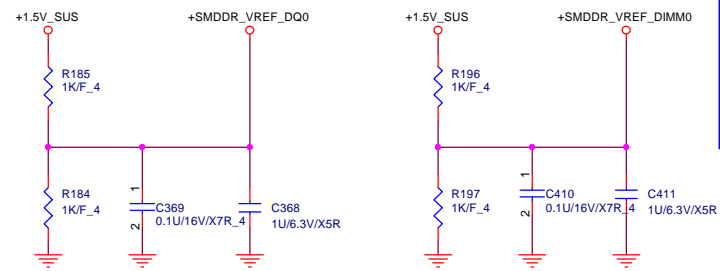
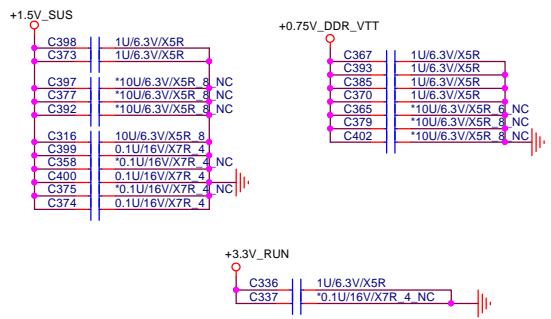


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL  Setting	DISABLE ILA AUTORUN  Setting	USE FC PLL  Setting	USE DEFAULT PCIe STRAPS  Setting	DISABLE PCI MEM BOOT  Setting
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIe STRAPS	ENABLE PCI MEM BOOT

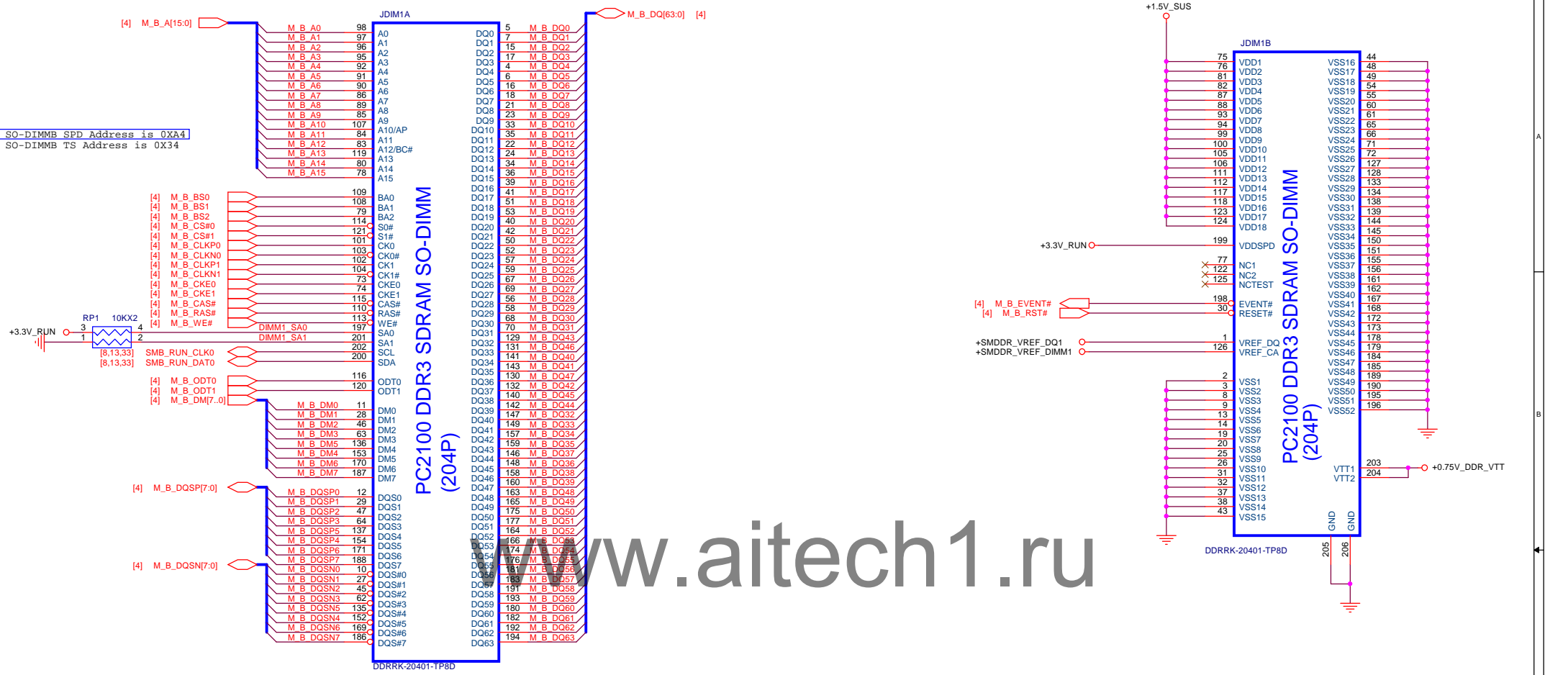




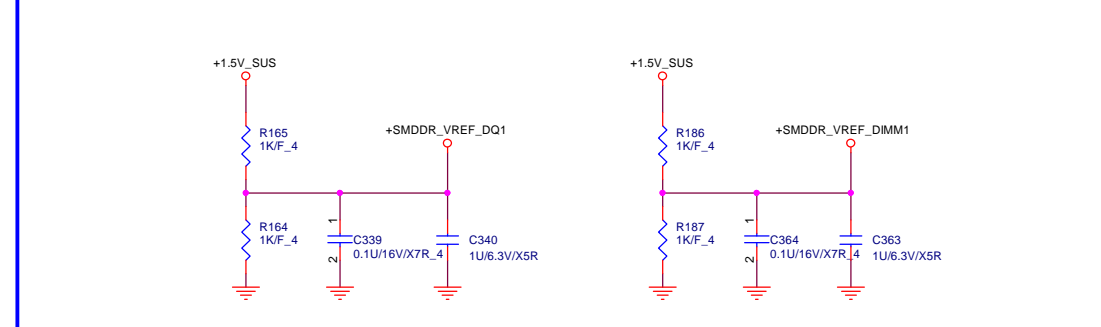
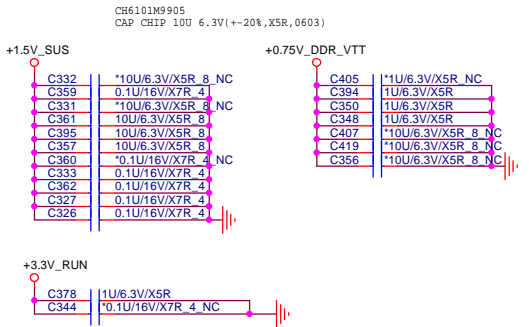
Place these Caps near So-Dimm0.

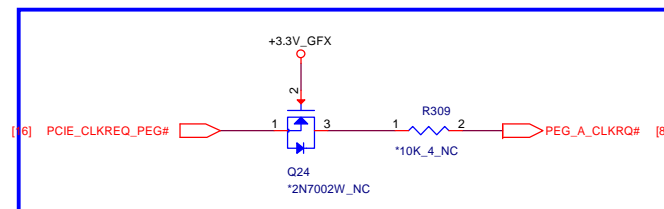
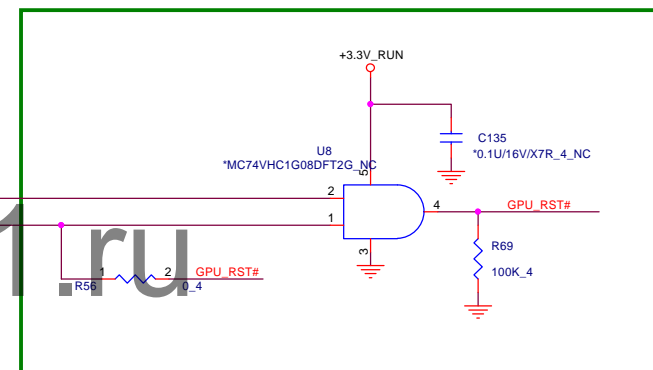
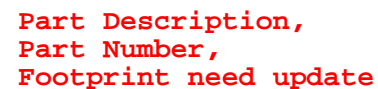


SO-DIMMB SPD Address is 0XA4  
SO-DIMMB TS Address is 0X34

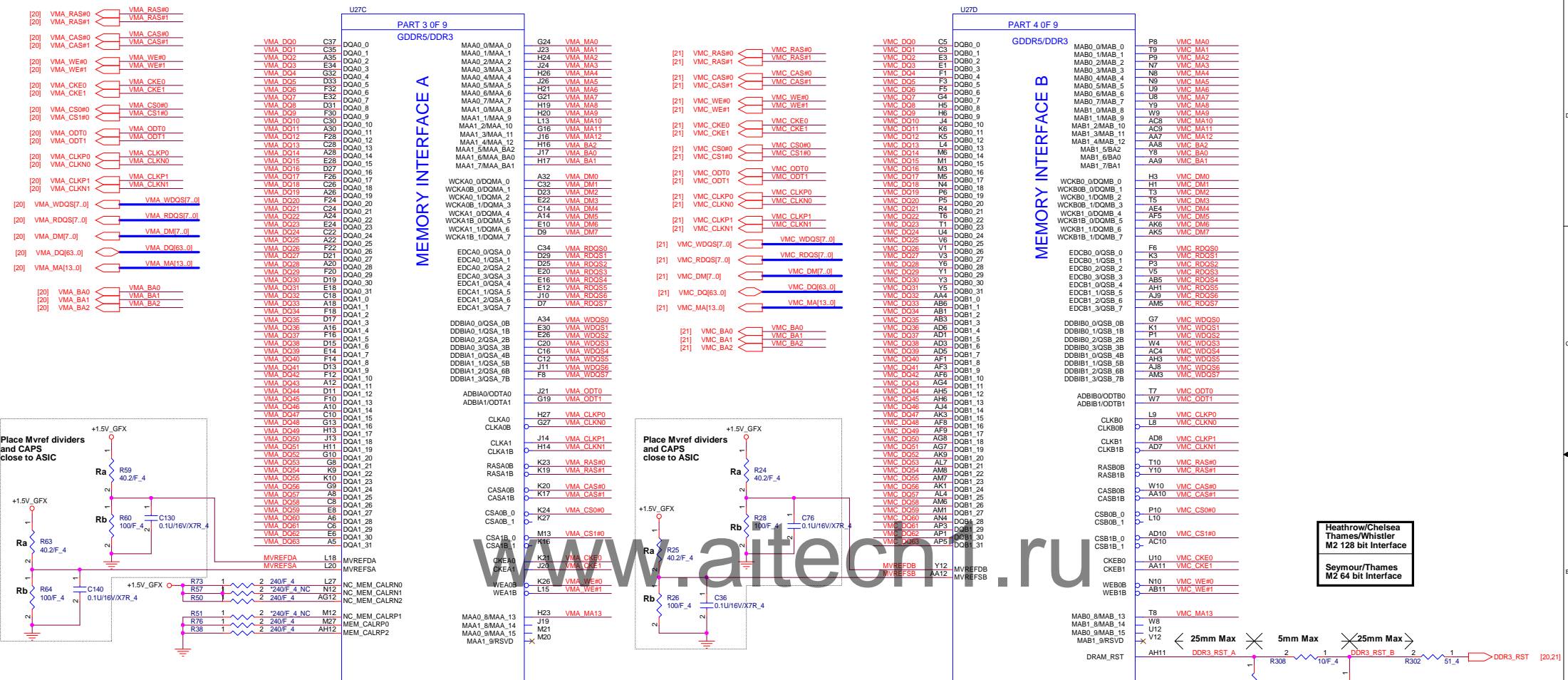


### Place these Caps near So-Dimm1.










	L27	N12	AG12	M12	M27	AH12
Heathrow/Chelsea	NC	NC	NC	NC	Stuff 120	Stuff 120
Thames/Whistler	Stuff 240	NC	Stuff 240	NC	Stuff 240	Stuff 240
Seymour	NC	Stuff 240	NC	Stuff 240	NC	NC

GPU (Pkg)	Preliminary Branding*	Memory Size	Mem Width	Memory Type	Mem Devices	Pro Perf (TDP)*	XT Perf (TDP)*
Chelsea (M2)	HD 7700	2 GB	128bit	128M x16 DDR3	8 pcs	P5500 (25W)	P5800 (35W)
	HD 7700	1 GB	128bit	64M x16 DDR3	8 pcs	P5500 (25W)	P5800 (35W)
Thames (M2)	HD 7600	2GB	128bit	128M x16 DDR3	8 pcs	P4600 (18W)	P5200 (22W)
	HD 7600	1GB	128-bit	64M x16 DDR3	8 pcs	P4600 (18W)	P5200 (22W)
	HD 7500	1GB	64-bit	128M x16 DDR3	4 pcs	P3000 (15W)	P3200 (18W)

GPU (Pkg)	Series Branding*	Mem Size	Mem width	Mem Type	Mem Devices	Pro Perf (TDP)*	XT Perf (TDP)*
Thames (M2)	HD 7600	1 GB	64-bit	128Mx16 GDDR5	(4pcs)	P3800 (18W)	-
	HD 7700	2 GB	128-bit	128Mx16 GDDR5	(8 pcs)	P6600 (25W)	P7500 (35W)
Chelsea (M2)	HD 7700	1 GB	128-bit	64Mx16 GDDR5	(8 pcs)	P6600 (25W)	P7500 (35W)
	HD 7800	2 GB	128-bit	128Mx16 GDDR5	(8 pcs)	P8000 (35W)	P9500 (45W)
Heathrow (M2)	HD 7800	1 GB	128-bit	64Mx16 GDDR5	(8 pcs)	P8000 (35W)	P9500 (45W)

GPU	Series Branding*	Mem Size	Mem width	Mem Type	Mem Devices	Pro Perf (TDP)*	XT Perf (TDP)*
Seymour GTX (M2)	HD 7400	512 MB	64-bit	64Mx32 GDDR5	(2pcs)	P2700 (20W)	-
	HD 7600	1 GB	128-bit	64Mx32 GDDR5	(4pcs)	P5200 (22W)	-
Thames (M2)	HD 7600	512 MB	64-bit	64Mx32 GDDR5	(2pcs)	P3800 (18W)	P4200 (25W)
	HD 7700	1GB	128-bit	64Mx32 GDDR5	(4pcs)	P6600 (25W)	P7500 (35W)
Chelsea (M2)	HD 7700	512 MB	128-bit	32Mx32 GDDR5	(4pcs)	P6600 (25W)	P7500 (35W)
	HD 7800	1GB	128-bit	64Mx32 GDDR5	(4pcs)	P8000 (35W)	P9500 (45W)



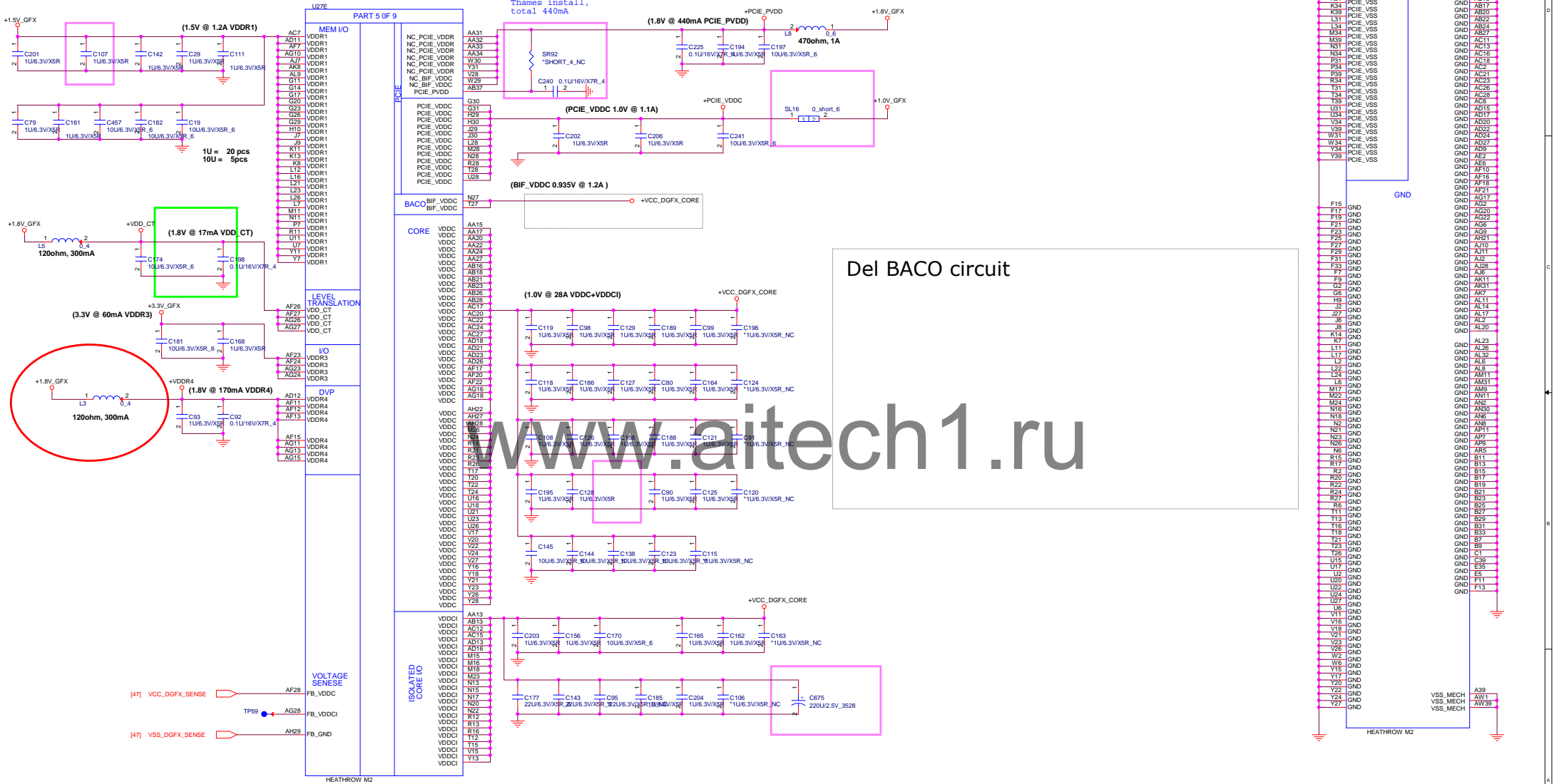
**Quanta Computer Inc.**  
**PROJECT : R0AA**

Size	Document Number	London_MEMORY	Rev	B
Date:	Monday, June 25, 2012	Sheet	17	of 55

For Thames/Whistler/Seymour  
NC\_PCIE\_VDDR and NC\_BIF\_VDDC  
should be tied with PCIE\_PVDD  
consumption about 440mA

Chelsea uninstall  
Thames install,  
total 440mA

Del BACO circuit







```
[17] VMA_MA[13..0]
[17] VMA_DQ[63..0]
[17] VMA_DM[7..0]
[17] VMA_WDQS[7..0]
[17] VMA_RDQS[7..0]
```



**VMA\_CLKP0** R86 2 1 56 4 C216 1 2 \*0.01U/25V/X7R\_4 NC

**VMA\_CLKN0** R85 2 1 56 4

**VMA\_CLKP1** R307 2 1 56 4

**VMA\_CLKN1** R312 2 1 56 4 C497 1 2 \*0.01U/25V/X7R\_4 NC

**+1.5V\_GFX** R75 1.33K/F\_4 VREFC\_VMA1 R79 1.33K/F\_4 C193 0.1U/16V/X7R\_4

**+1.5V\_GFX** R353 1.33K/F\_4 VREFD\_VMA1 R349 1.33K/F\_4 C515 0.1U/16V/X7R\_4

**+1.5V\_GFX** R49 1.33K/F\_4 VREFC\_VMA3 R45 1.33K/F\_4 C67 0.1U/16V/X7R\_4

**+1.5V\_GFX** R36 1.33K/F\_4 VREFD\_VMA3 R39 1.33K/F\_4 C53 0.1U/16V/X7R\_4

**+1.5V\_GFX** C26 22U/4V/X6S\_8 C676 22U/4V/X6S\_8

**+1.5V\_GFX** C674 10U/6.3V/X5R\_8 C673 10U/6.3V/X5R\_8 C33 1 2 \*1U/6.3V/X5R NC C37 1 2 1U/6.3V/X5R C157 1 2 1U/6.3V/X5R C40 1 2 1U/6.3V/X5R C213 1 2 0.1U/16V/X7R\_4 C141 1 2 0.1U/16V/X7R\_4 C152 1 2 0.1U/16V/X7R\_4 C39 1 2 0.1U/16V/X7R\_4 C46 1 2 0.1U/16V/X7R\_4 C175 1 2 \*0.1U/16V/X7R\_4 NC

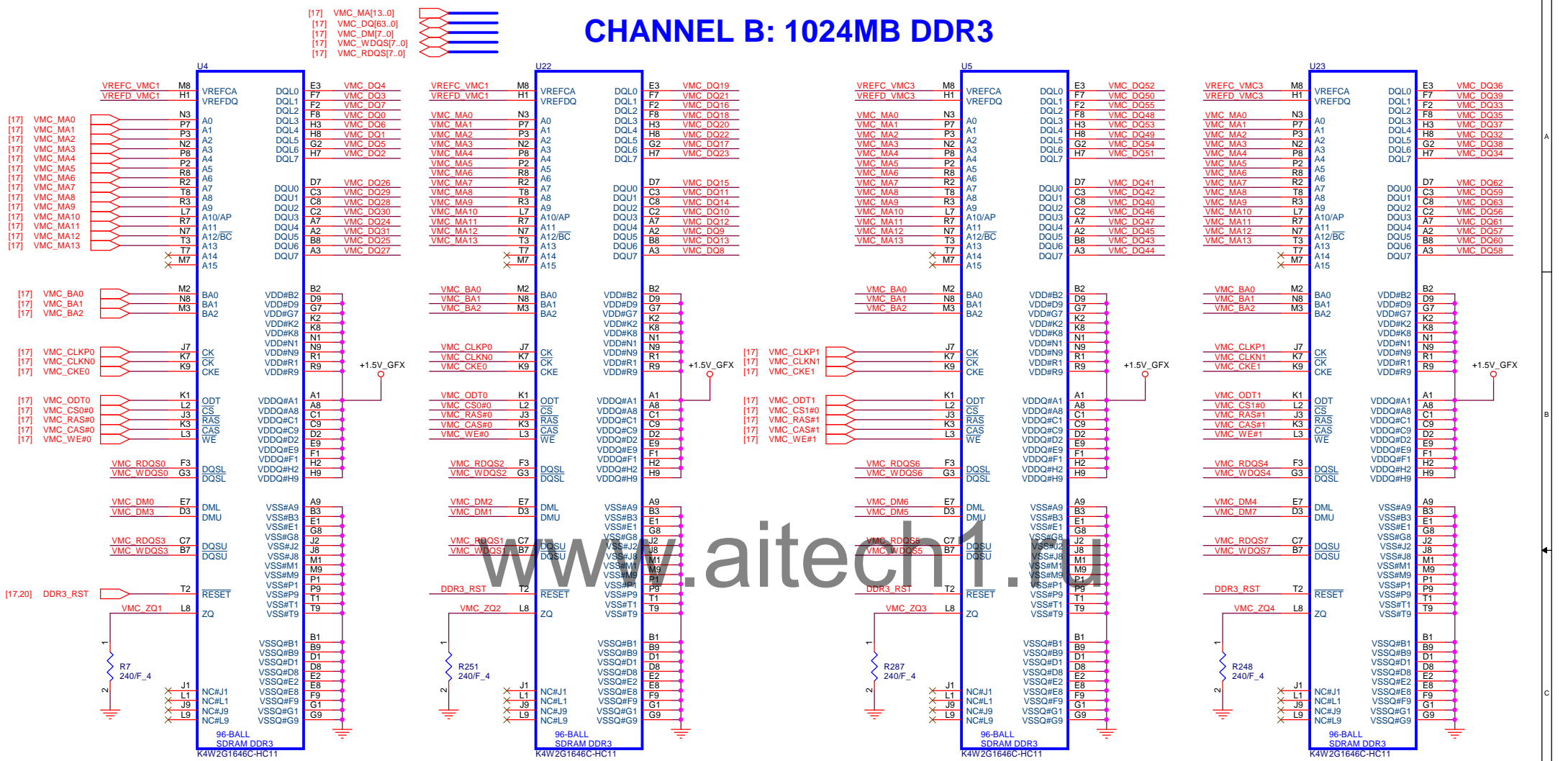
**+1.5V\_GFX** C83 1 2 \*1U/6.3V/X5R NC C80 1 2 1U/6.3V/X5R C105 1 2 1U/6.3V/X5R C112 1 2 0.1U/16V/X7R\_4 C217 1 2 0.1U/16V/X7R\_4 C27 1 2 0.1U/16V/X7R\_4 C221 1 2 0.1U/16V/X7R\_4 C218 1 2 0.1U/16V/X7R\_4 C222 1 2 \*0.1U/16V/X7R\_4 NC

**+1.5V\_GFX** C506 1 2 \*1U/6.3V/X5R NC C507 1 2 1U/6.3V/X5R C505 1 2 1U/6.3V/X5R C510 1 2 1U/6.3V/X5R C509 1 2 0.1U/16V/X7R\_4 C512 1 2 0.1U/16V/X7R\_4 C528 1 2 0.1U/16V/X7R\_4 C517 1 2 0.1U/16V/X7R\_4 C516 1 2 0.1U/16V/X7R\_4 C519 1 2 \*0.1U/16V/X7R\_4 NC

**+1.5V\_GFX** C492 1 2 \*1U/6.3V/X5R NC C503 1 2 1U/6.3V/X5R C493 1 2 1U/6.3V/X5R C494 1 2 1U/6.3V/X5R C495 1 2 0.1U/16V/X7R\_4 C500 1 2 0.1U/16V/X7R\_4 C504 1 2 0.1U/16V/X7R\_4 C499 1 2 0.1U/16V/X7R\_4 C501 1 2 0.1U/16V/X7R\_4 C502 1 2 \*0.1U/16V/X7R\_4 NC

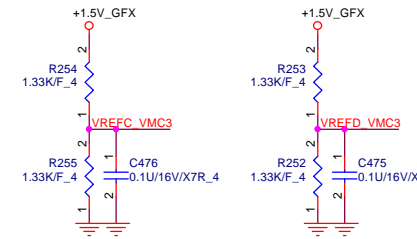
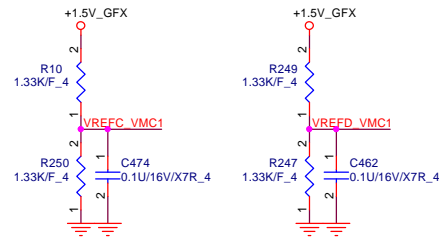
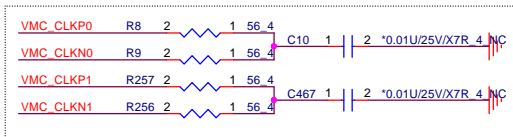


# CHANNEL B: 1024MB DDR3



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Placement has to be close to VRAM



C11	1	2	*1U/6.3V/X5R	NC
C12	1	2	1U/6.3V/X5R	
C9	1	2	1U/6.3V/X5R	
C8	1	2	1U/6.3V/X5R	
C473	1	2	0.1U/16V/X7R_4	
C34	1	2	0.1U/16V/X7R_4	
C38	1	2	0.1U/16V/X7R_4	
C35	1	2	0.1U/16V/X7R_4	
C22	1	2	0.1U/16V/X7R_4	
C24	1	2	0.1U/16V/X7R_4	NC

C16	1	2	*1U/6.3V/X5R	NC
C7	1	2	1U/6.3V/X5R	
C21	1	2	1U/6.3V/X5R	
C6	1	2	1U/6.3V/X5R	
C5	1	2	0.1U/16V/X7R_4	
C30	1	2	0.1U/16V/X7R_4	
C31	1	2	1U/6.3V/X5R	
C14	1	2	0.1U/16V/X7R_4	
C13	1	2	0.1U/16V/X7R_4	
C15	1	2	0.1U/16V/X7R_4	NC

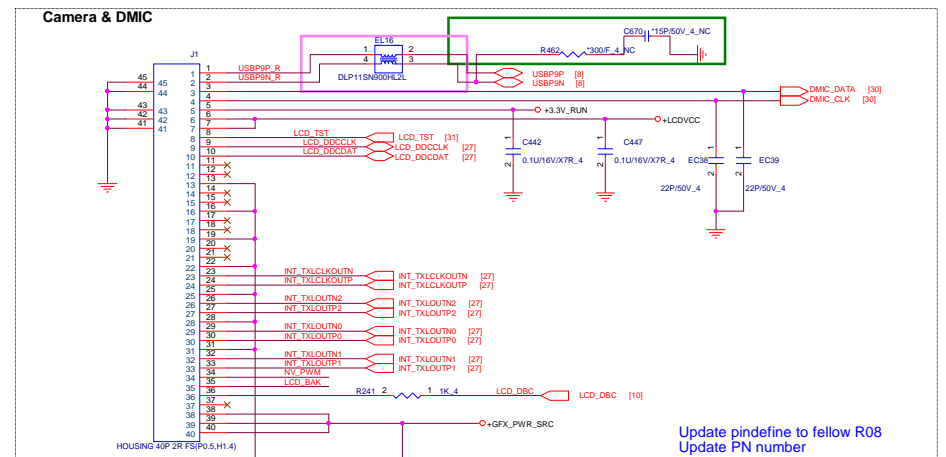
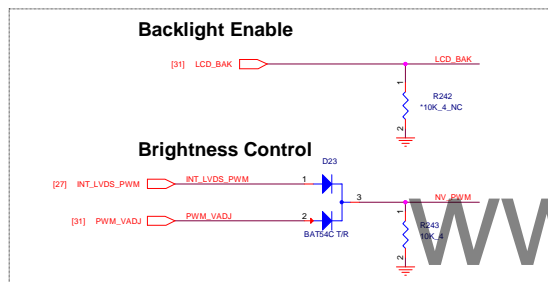
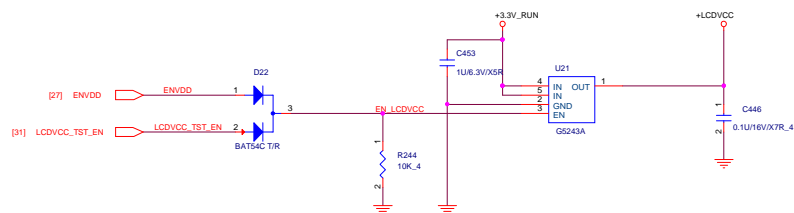
C489	1	2	*1U/6.3V/X5R	NC
C465	1	2	1U/6.3V/X5R	
C479	1	2	1U/6.3V/X5R	
C464	1	2	1U/6.3V/X5R	
C487	1	2	0.1U/16V/X7R_4	
C481	1	2	0.1U/16V/X7R_4	
C471	1	2	0.1U/16V/X7R_4	
C461	1	2	0.1U/16V/X7R_4	
C458	1	2	0.1U/16V/X7R_4	
C469	1	2	0.1U/16V/X7R_4	NC

C470	1	2	*1U/6.3V/X5R	NC
C466	1	2	1U/6.3V/X5R	
C463	1	2	1U/6.3V/X5R	
C459	1	2	1U/6.3V/X5R	
C468	1	2	0.1U/16V/X7R_4	
C480	1	2	0.1U/16V/X7R_4	
C472	1	2	0.1U/16V/X7R_4	
C491	1	2	0.1U/16V/X7R_4	
C477	1	2	0.1U/16V/X7R_4	
C460	1	2	0.1U/16V/X7R_4	NC



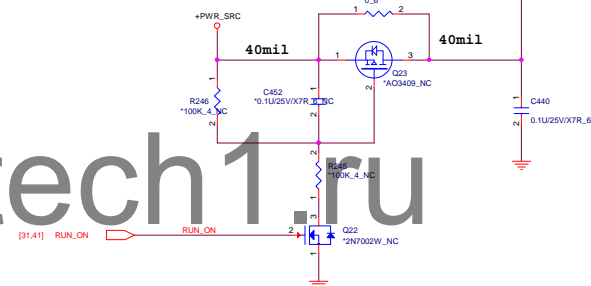
**Quanta Computer Inc.**  
PROJECT : R0AA

Size	Document Number	Rev
	N11M-GE2 VRAM-2(DDR3 BGA96)	1A
Date:	Monday, June 25, 2012	Sheet 21 of 55

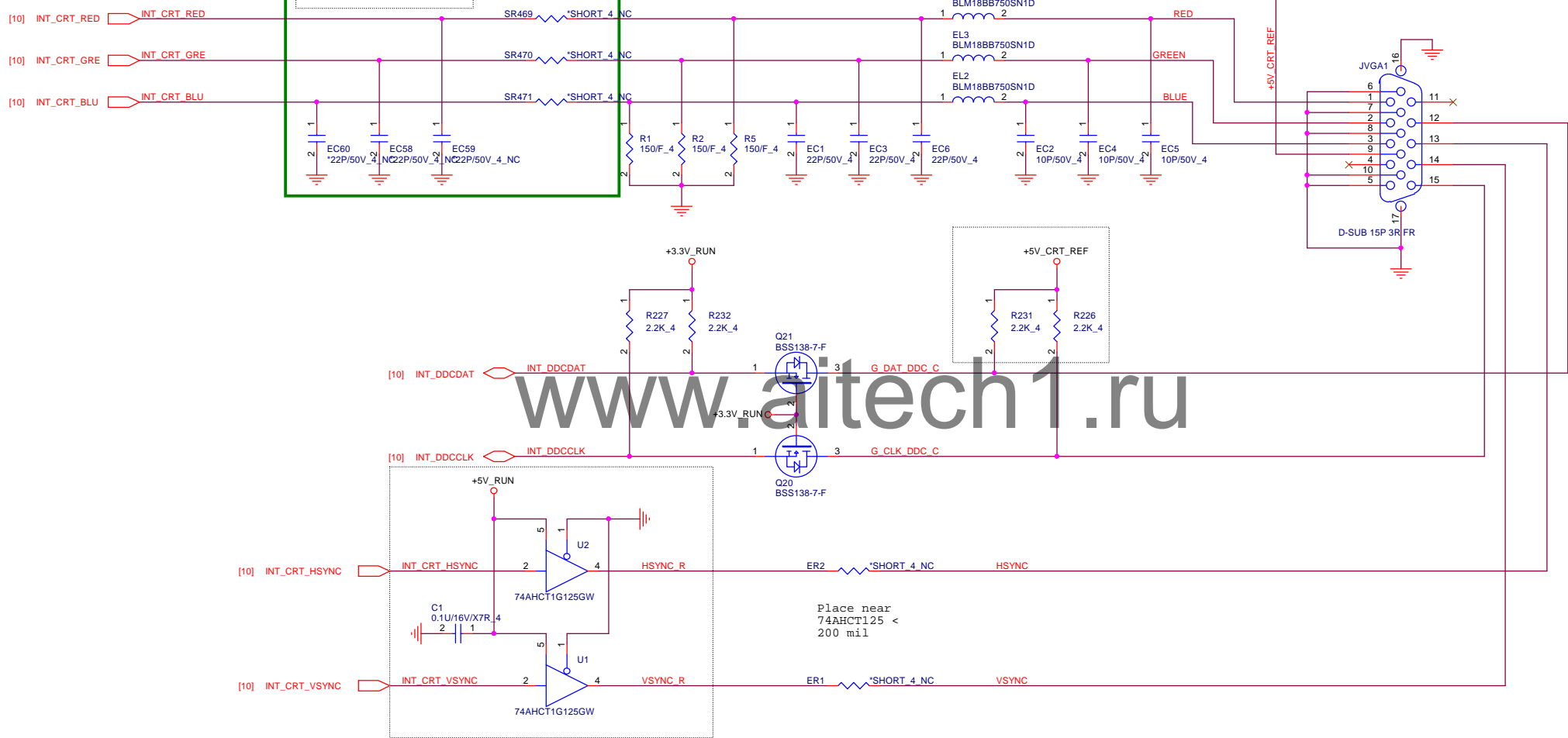


#### EMC Reserve

INT_TXCLKOUTN	ER18_1	2	3.3P	INT_TXCLKOUTP
INT_TXOUTN2	ER18_1	2	3.3P	INT_TXOUTP2
INT_TXOUTN1	ER17_1	2	3.3P	INT_TXOUTP1
INT_TXOUTN0	ER19_1	2	3.3P	INT_TXOUTP0



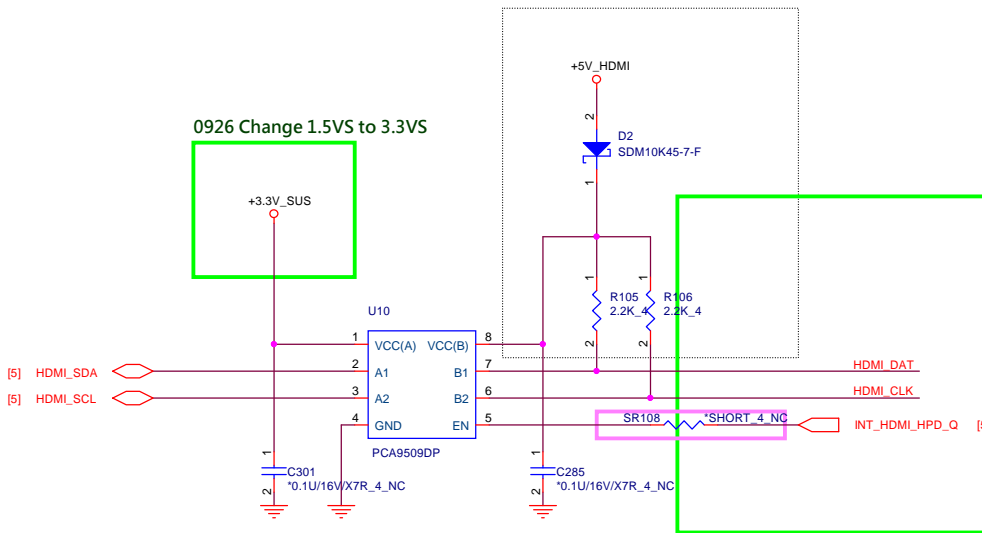
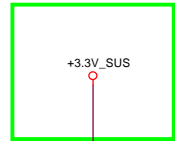
**Layout Note:**  
Setting R,G,B treac  
impedance to 50 ohm.



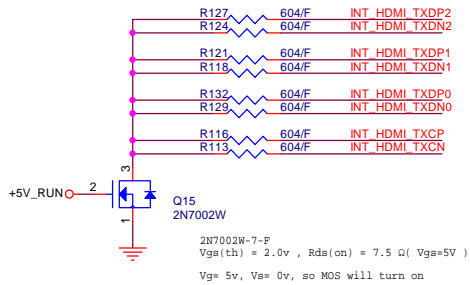
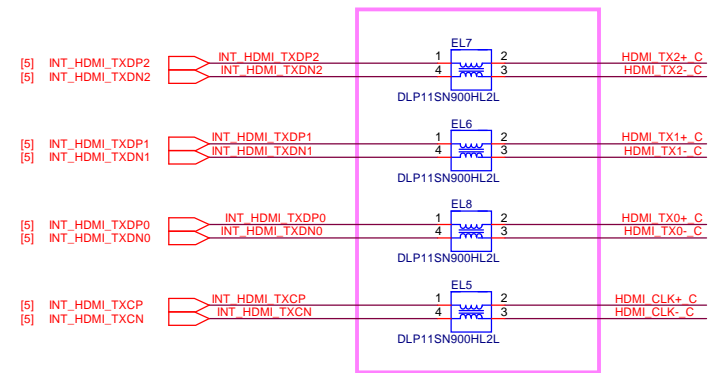
**Quanta Computer Inc.**  
**PROJECT : R0AA**

Size	Document Number	Rev
	<b>VGA Conn</b>	<b>B</b>
Date:	Friday, June 29, 2012	Sheet 23 of 55

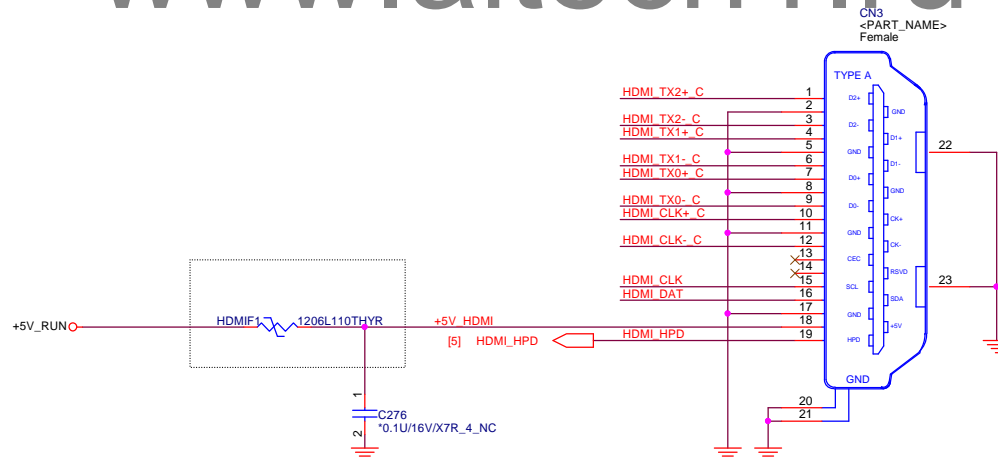
0926 Change 1.5VS to 3.3VS



Reserve for EMI and close to HDMI CONN



www.aitech1.ru HDMI Conn.

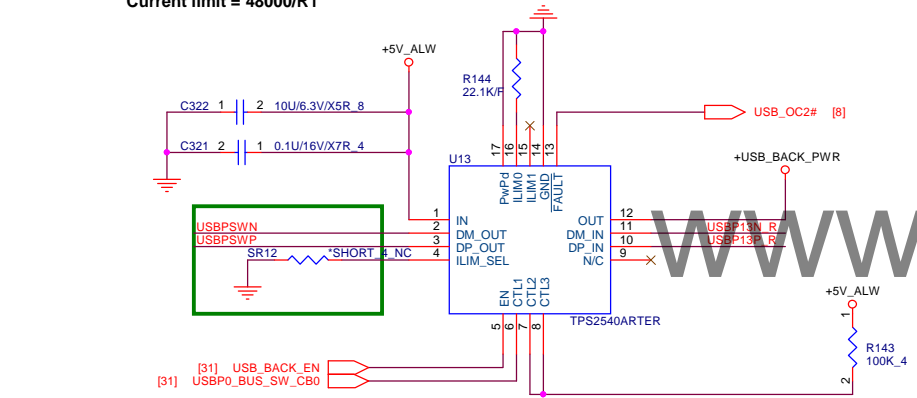
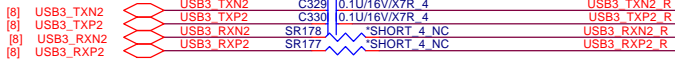
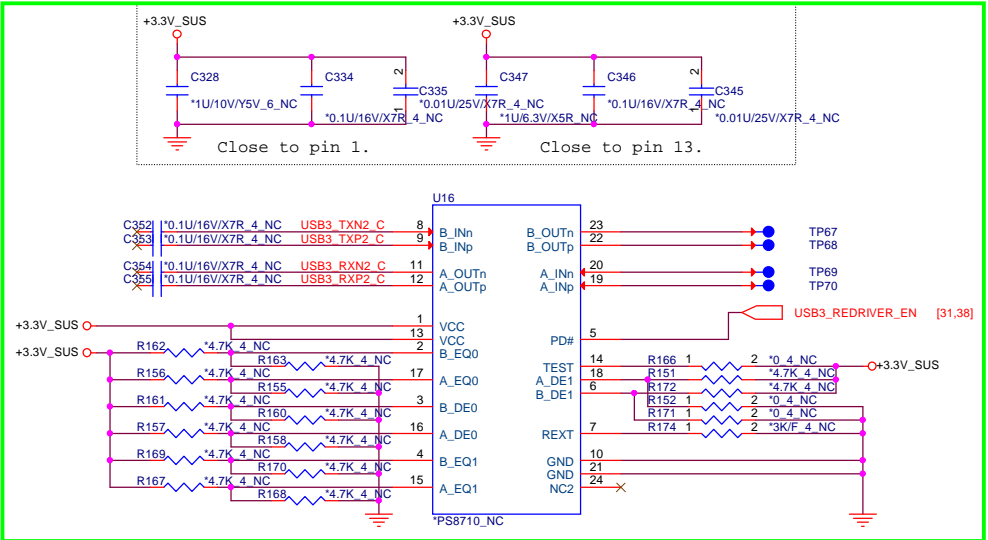
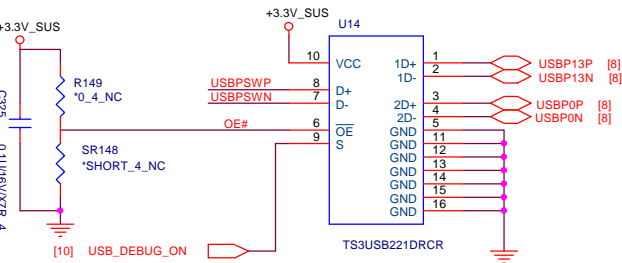


S	OE	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

## USB Power share

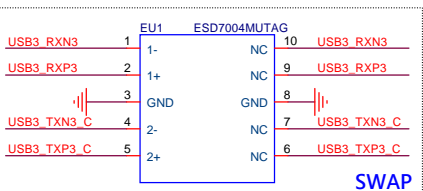
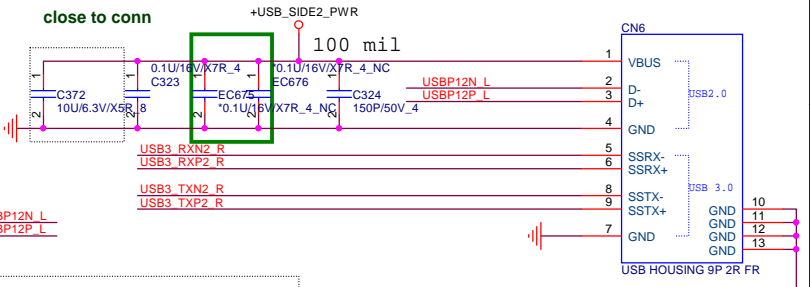
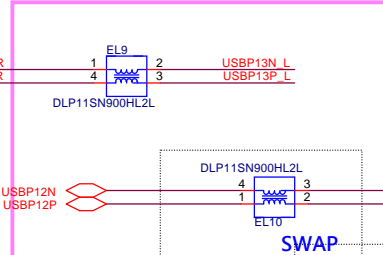
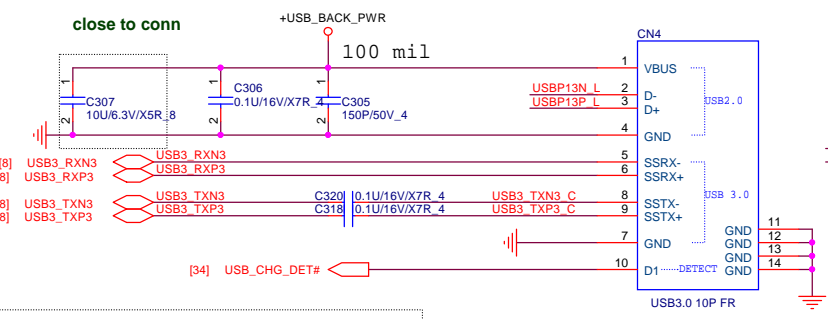
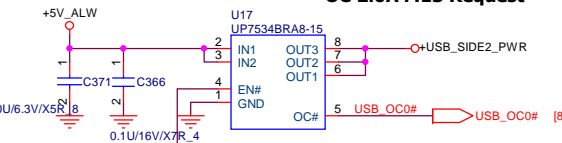
USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

OC limitation	R1	mA
	100k ohm	480
	22.1k ohm	2171

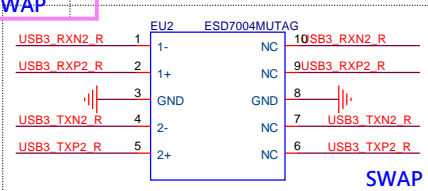
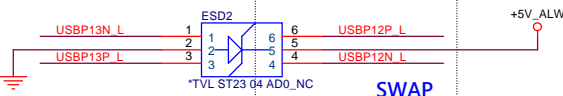


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I continuous 1.5A  
OC 2.0A M13 Request

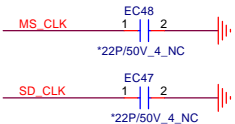
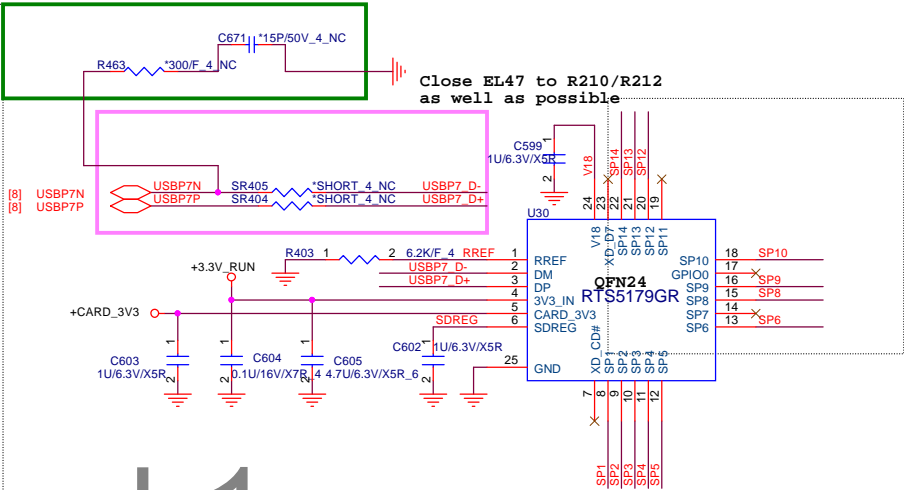
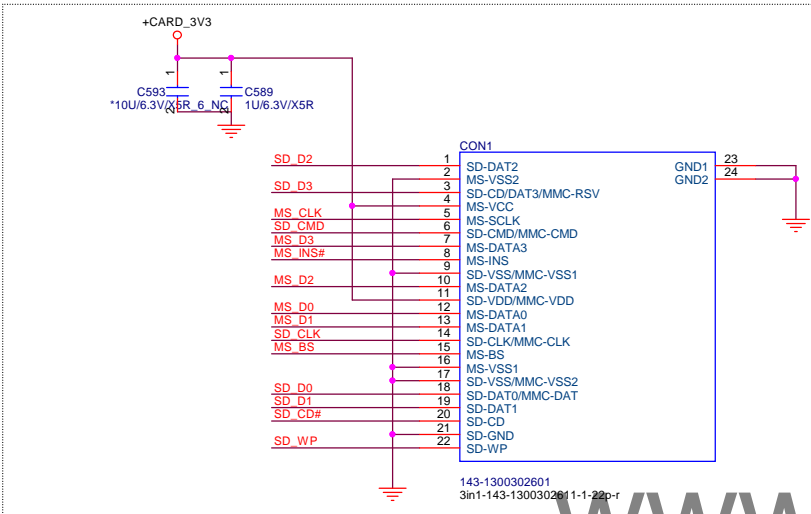


ESD Function  
Place ESD diodes as close as USB connector.



Cardreader (RTS5179GR) Support SD3.0 USH50

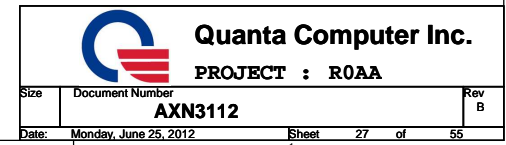
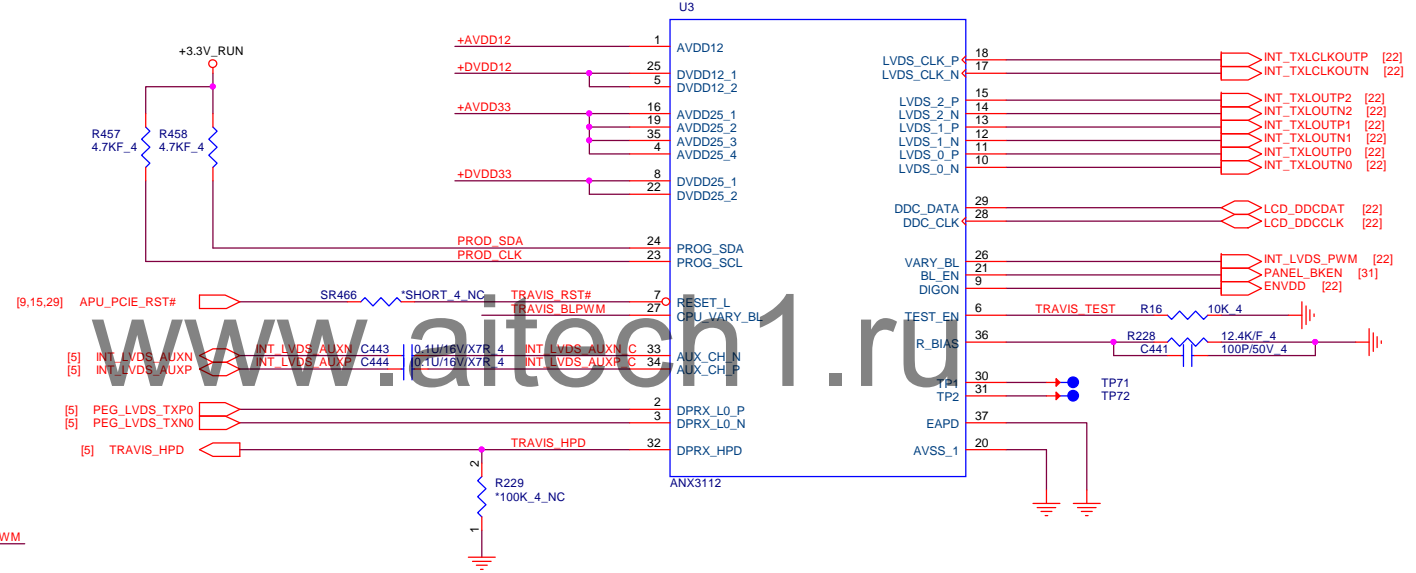
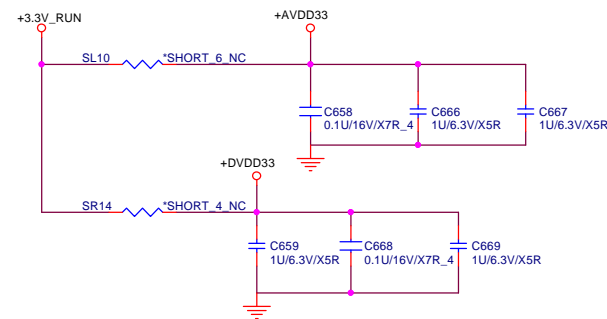
Change CON1 footprint to 3in1-143-1300302611-1-22p-r(follow R09)



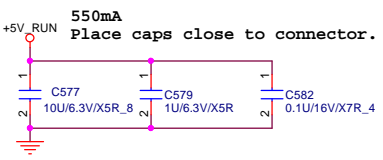
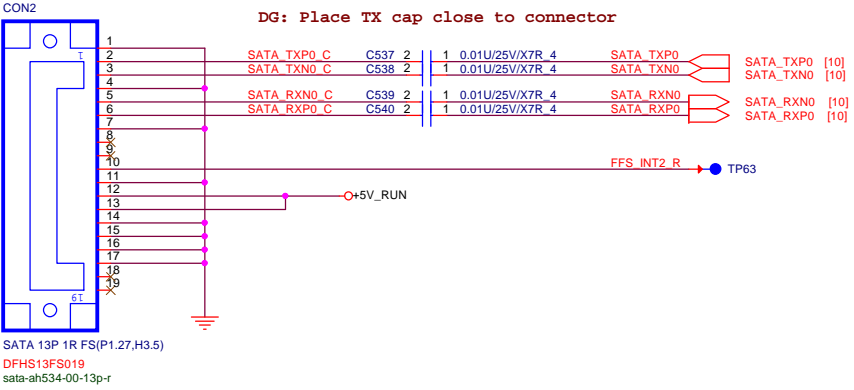
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Share Pin

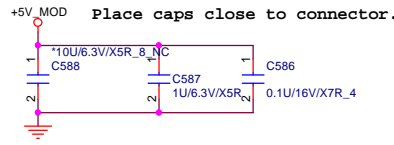
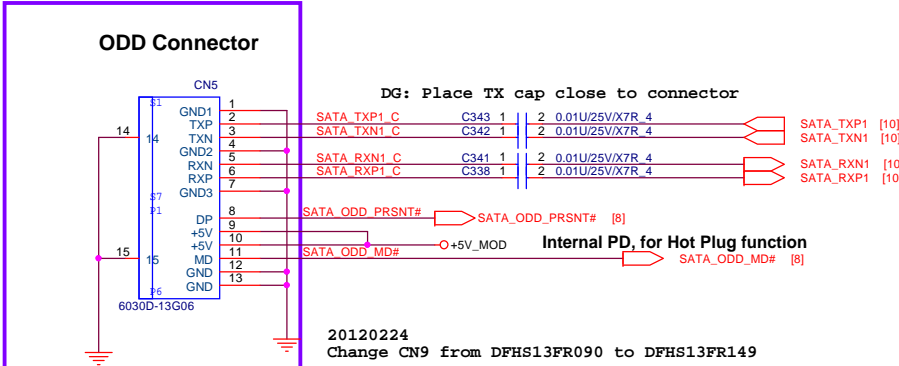
	SD_CARD	MS_CARD
SP1	SW_WP	MS_CLK
SP2		MS_INS#
SP3	SD_D1	
SP4	SD_D0	MS_D7
SP5	SD_D7	MS_D3
SP6	SD_CD#	
SP7	SD_D6	MS_D6
SP8	SD_CLK	MS_D2
SP9	SD_D5	MS_D0
SP10	SD_CMD	
SP11	SD_D4	MS_D4
SP12	SD_D3	MS_D1
SP13	SD_D2	MS_D5
SP14		MS_BS



HDD

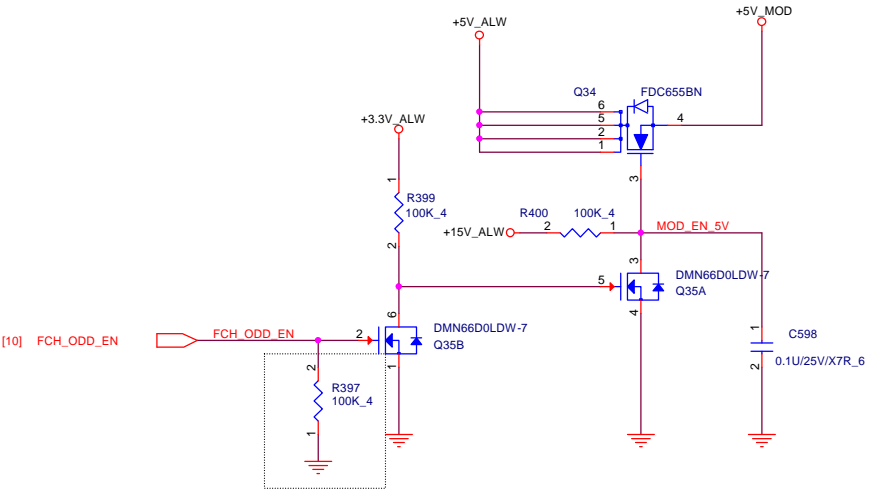


ODD

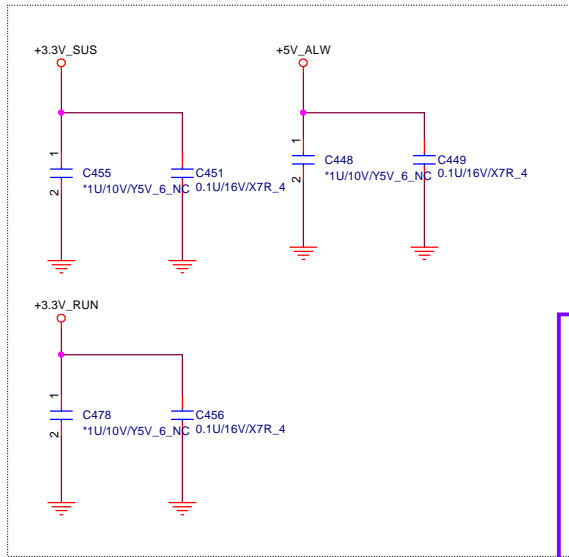


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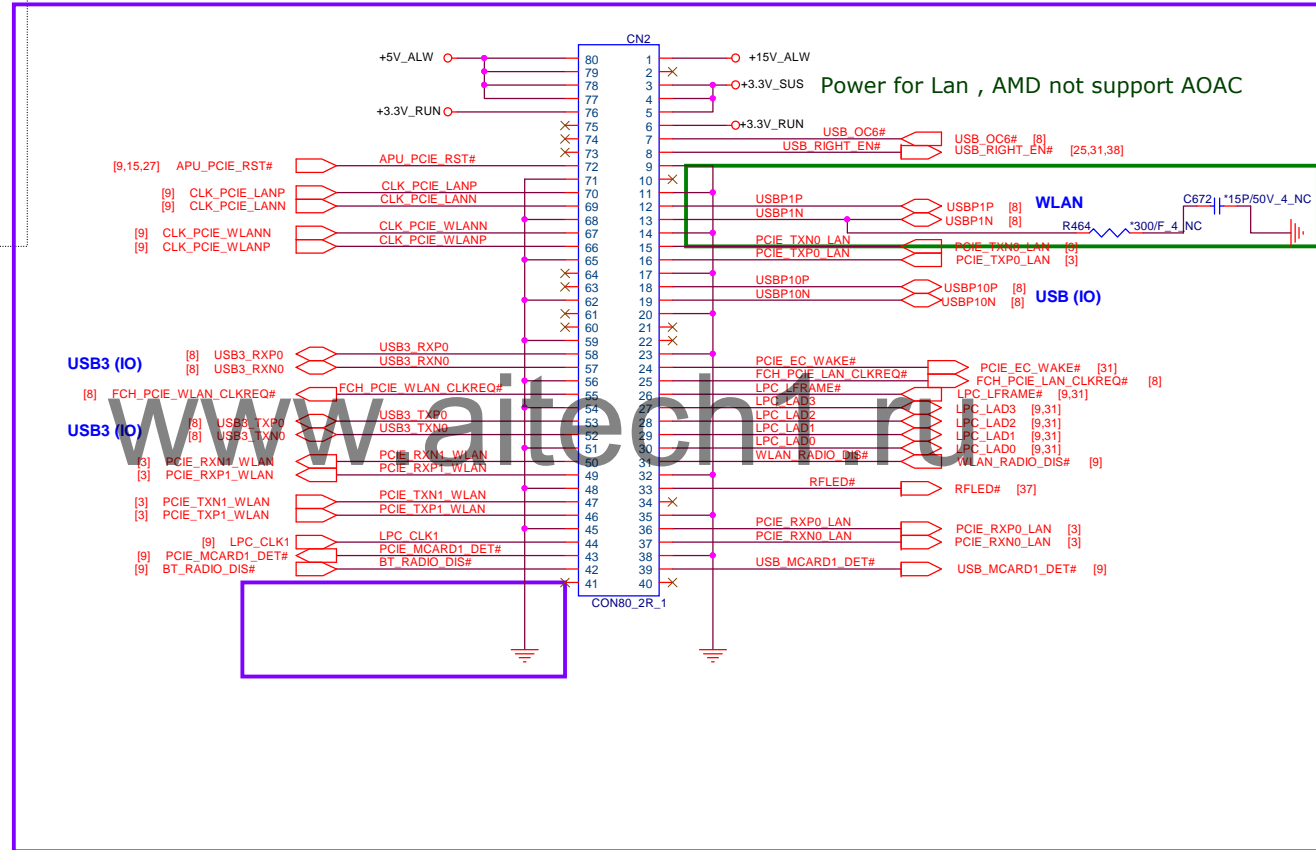
Support Zero power ODD



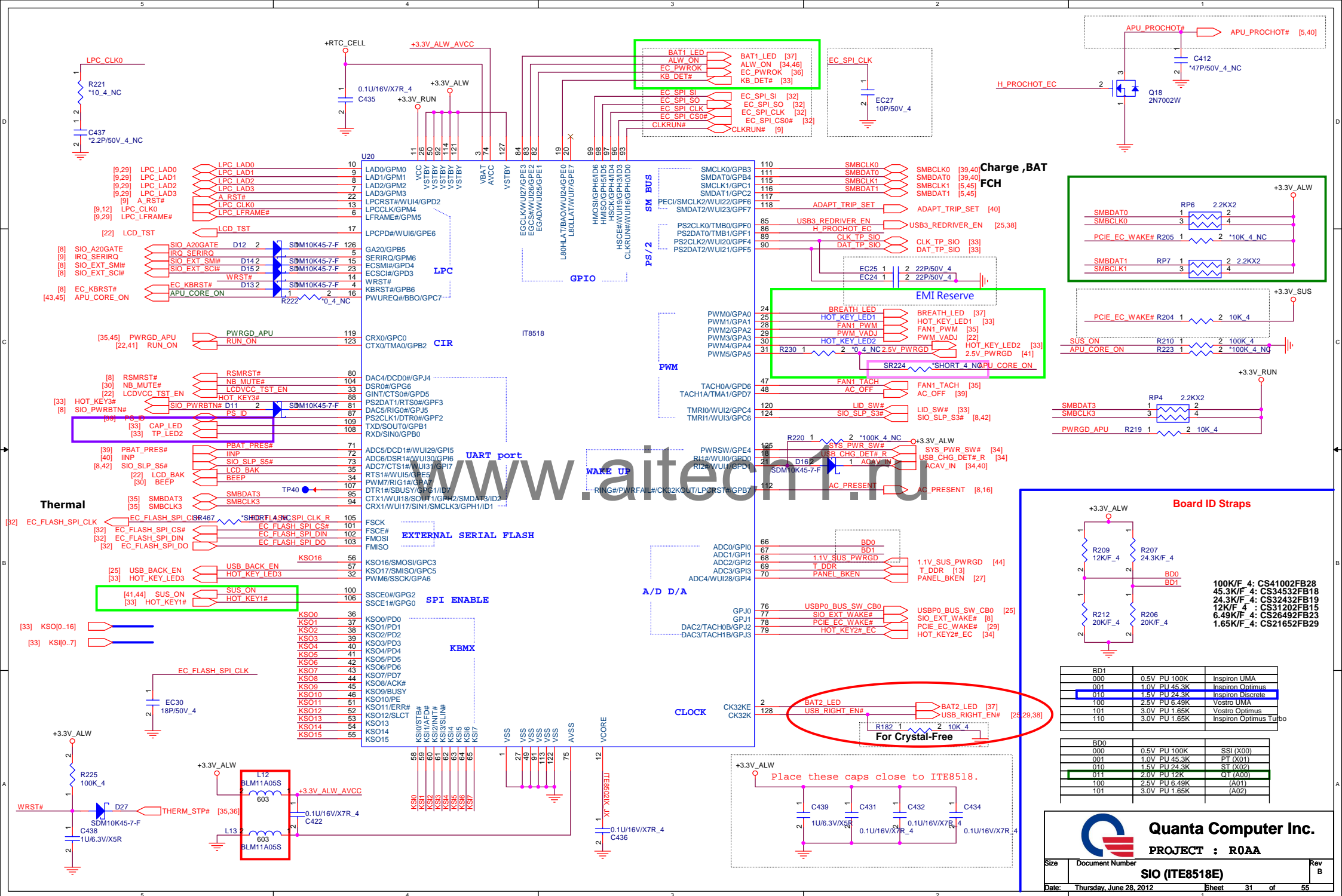




20120229  
Change CN9 footprint from "88161-08001-80p-ldh" to "88069-8001b-bs-80p-ldh-smt"

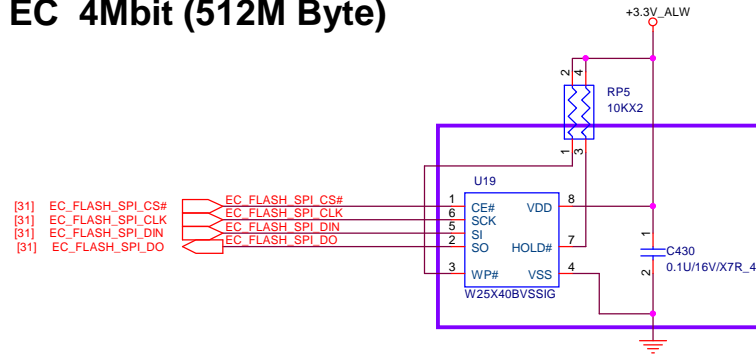




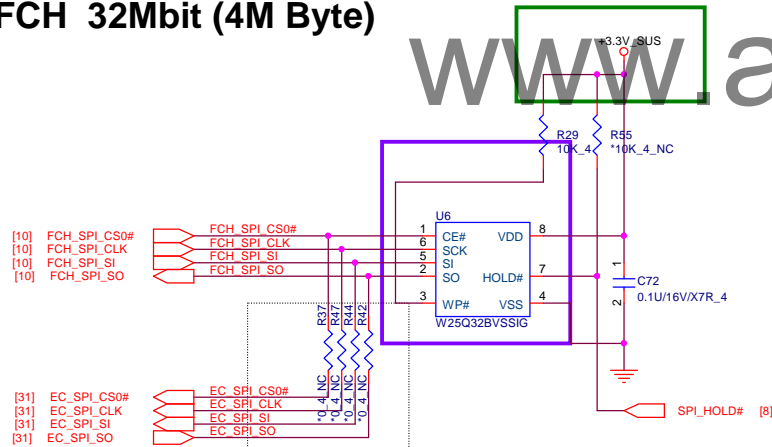


# FLASH / RTC

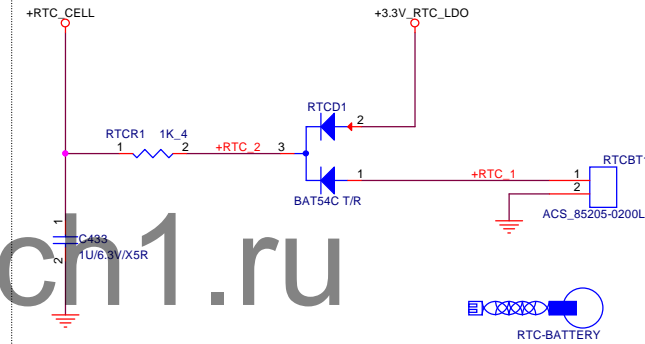
## For EC 4Mbit (512M Byte)



## For FCH 32Mbit (4M Byte)



## RTC



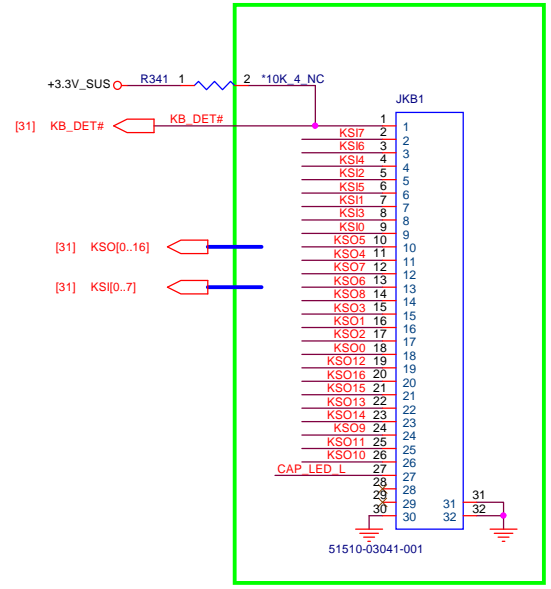
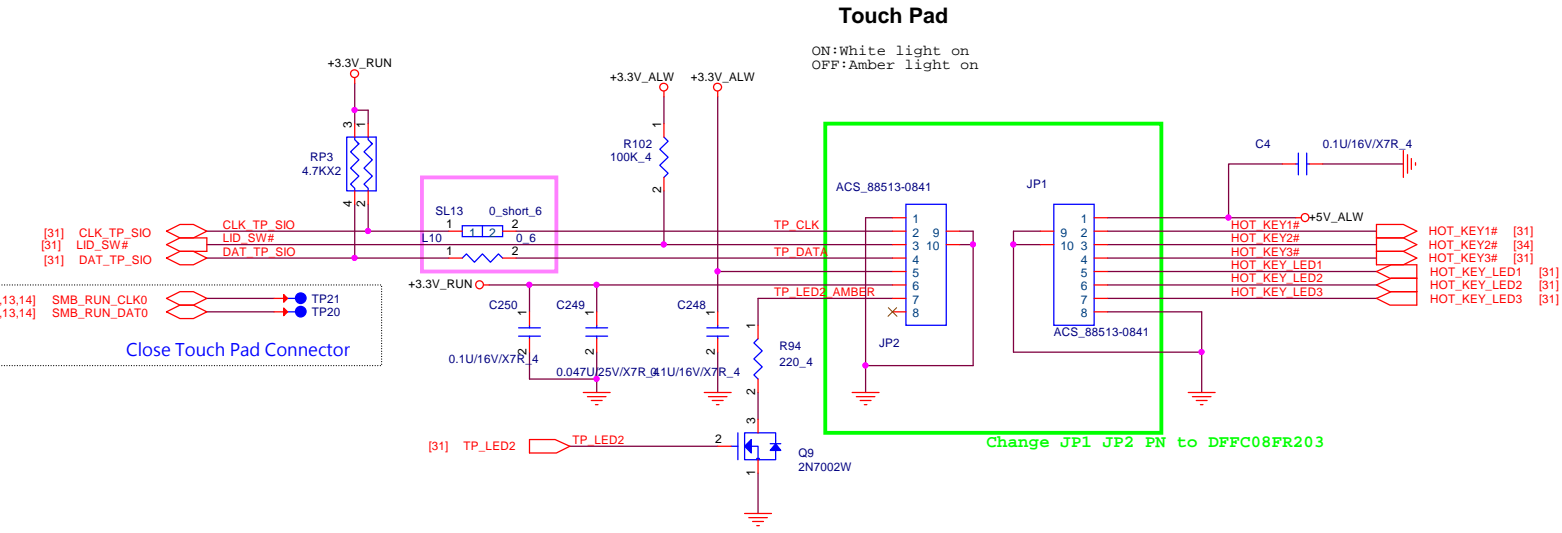
Double, 25'C, Vf=0.4V, If=25mA  
one, 25'C, Vf=0.35V, If=15.8mA



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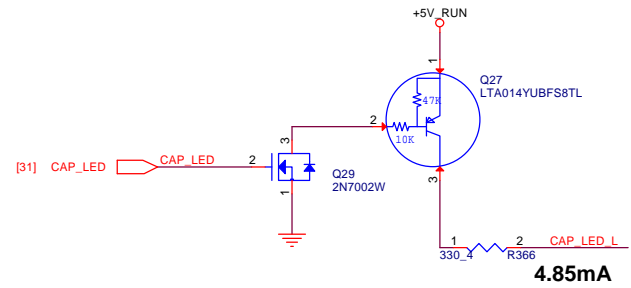
PROJECT : R0AA

# KEYBOARD CONNECTOR



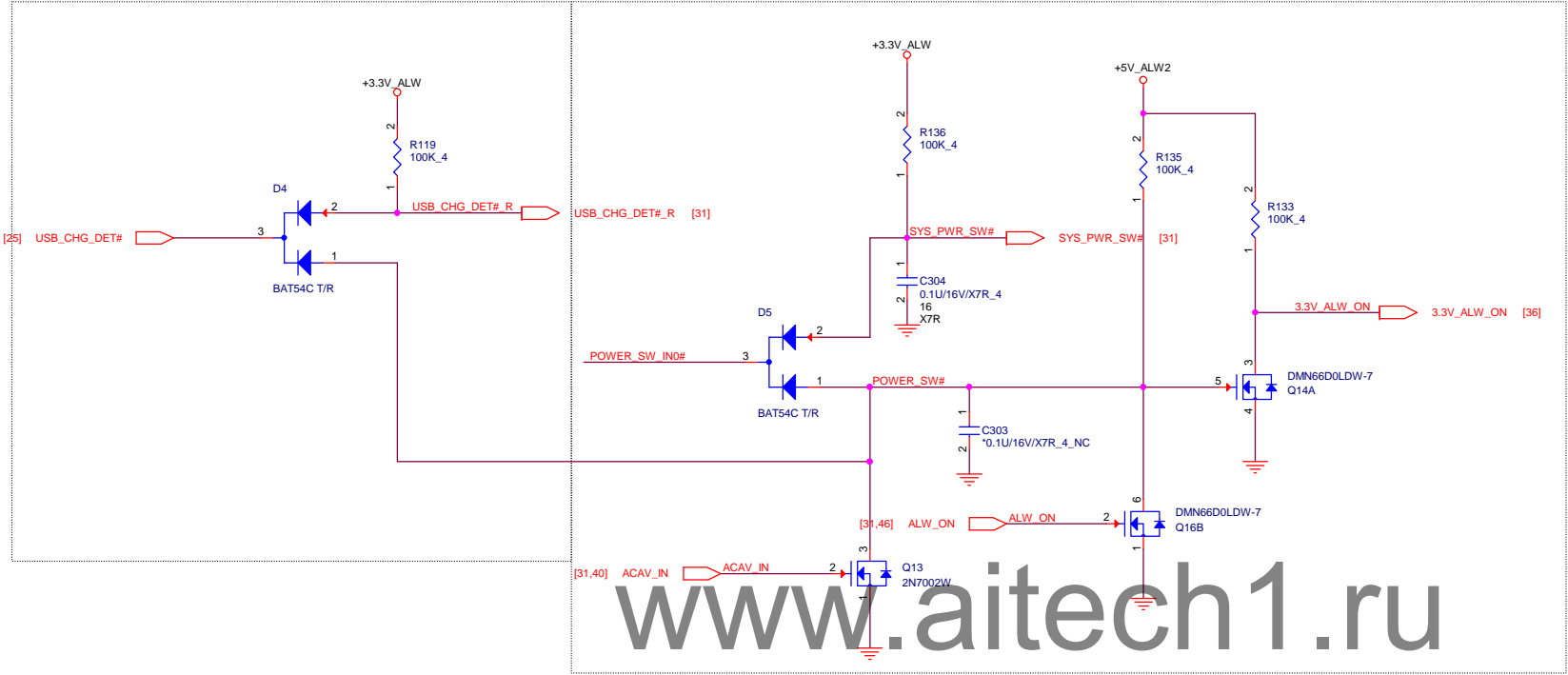
www.aitech1.ru

$V_{i(on\_max)} = -1.4V$   
 $V_{i(off\_min)} = -0.3$



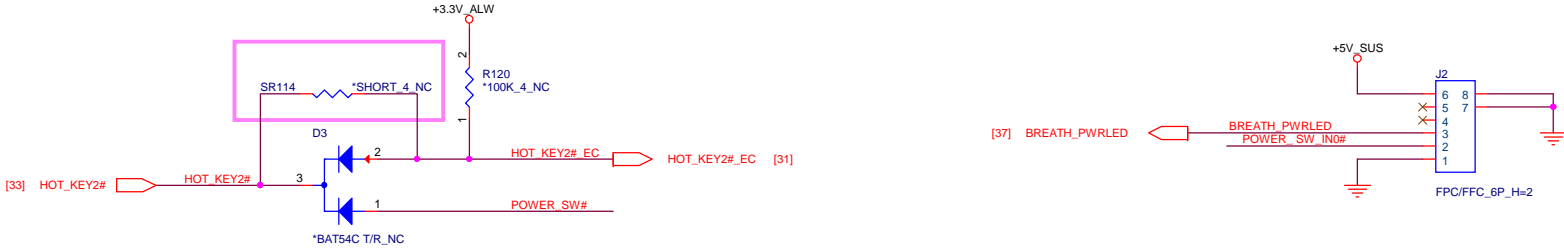
For USB charger usage

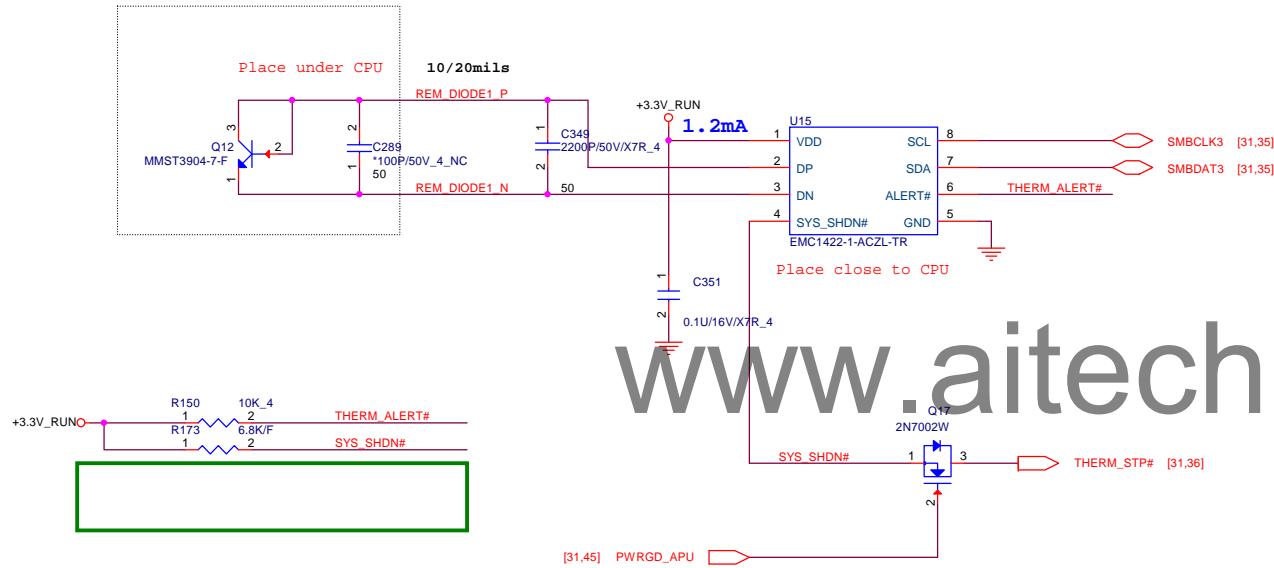
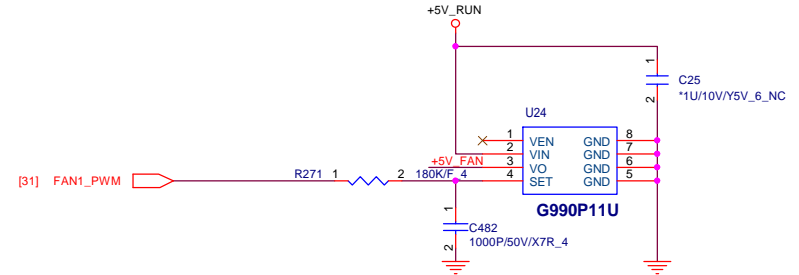
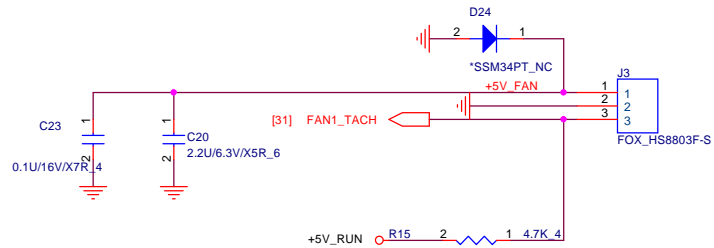
3V ALW ON POWER LOGIC



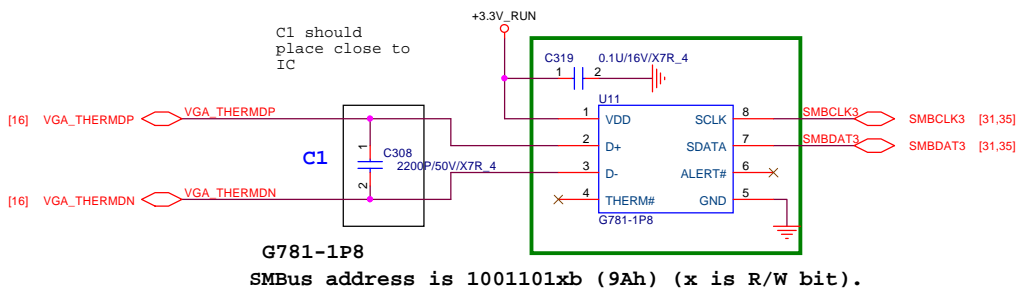
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TO PWR button board



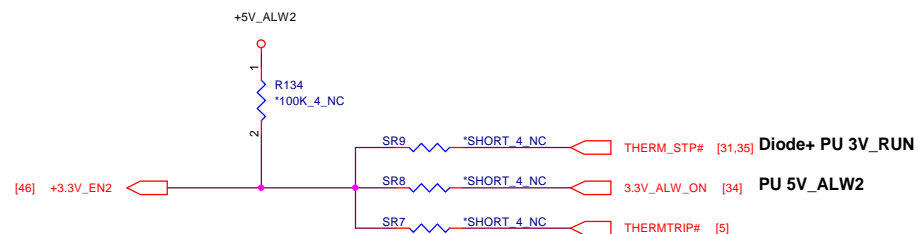
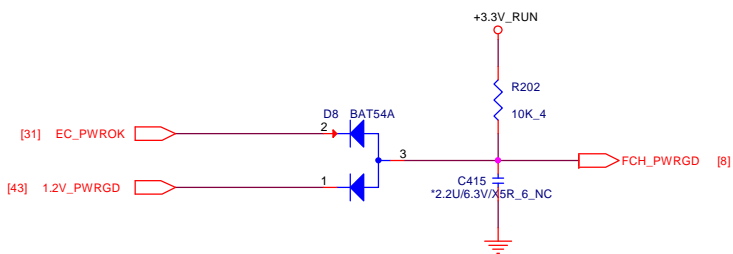


SYS_SHDN#	4.7K	6.8K	10K	15K	22K	33K
ALERT#						
4.7K	77°C	83°C	89°C	95°C	101°C	107°C
6.8K	78°C	84°C	90°C	96°C	102°C	108°C
10K	79°C	85°C	91°C	97°C	103°C	109°C
15K	80°C	86°C	92°C	98°C	104°C	110°C
22K	81°C	87°C	93°C	99°C	105°C	111°C
33K	82°C	88°C	94°C	100°C	106°C	112°C



G781-1P8

SMBus address is 1001101xb (9Ah) (x is R/W bit).



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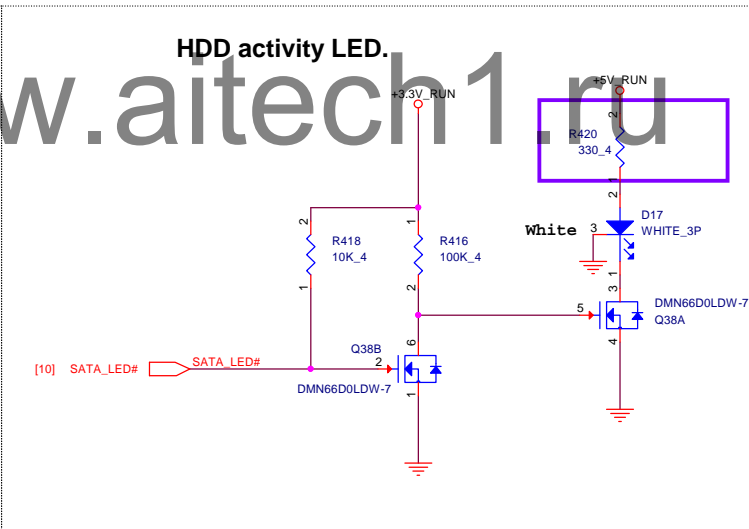
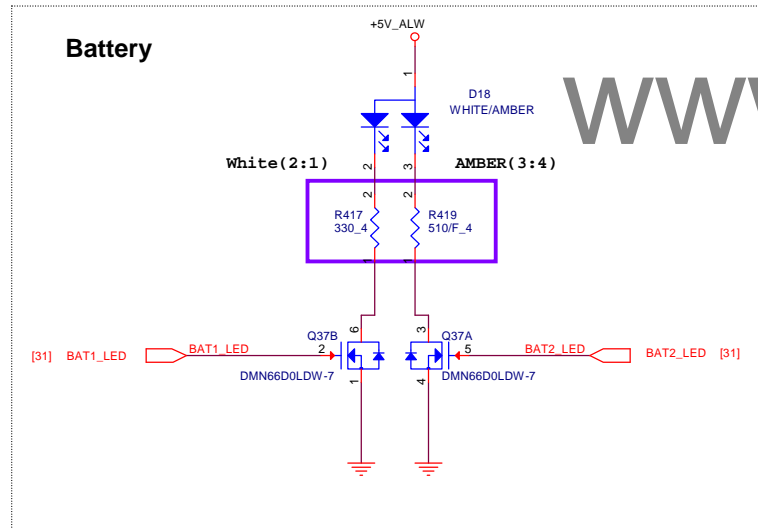
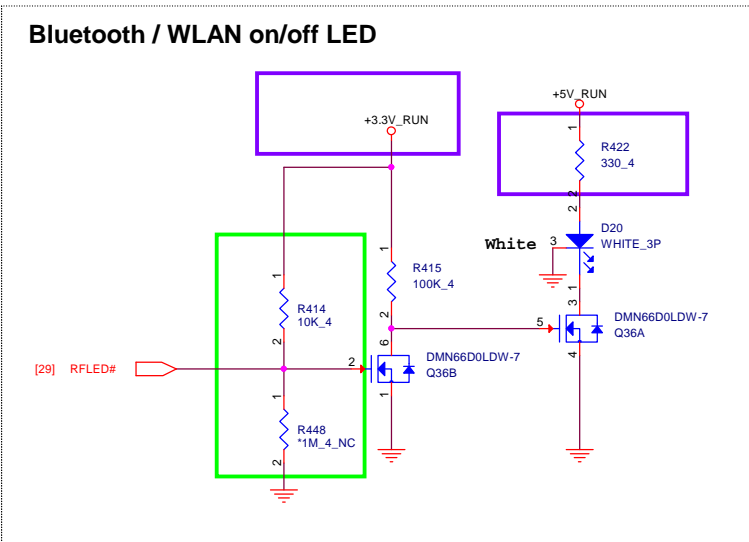
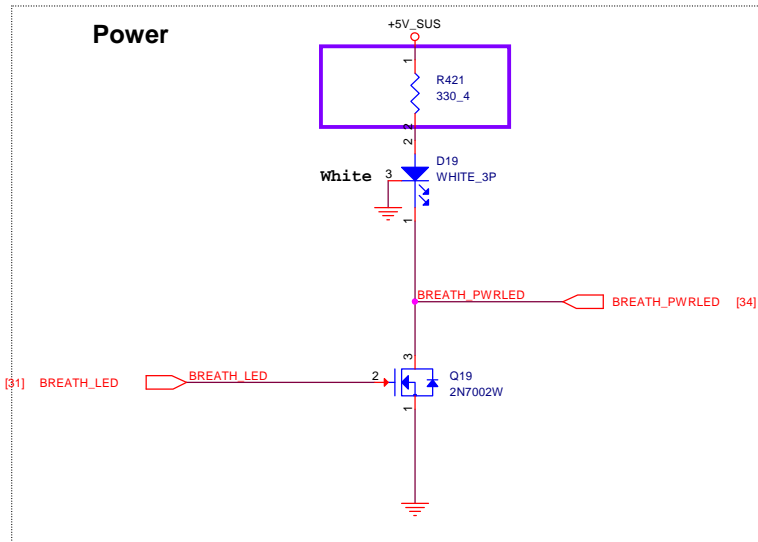
**Quanta Computer Inc.**

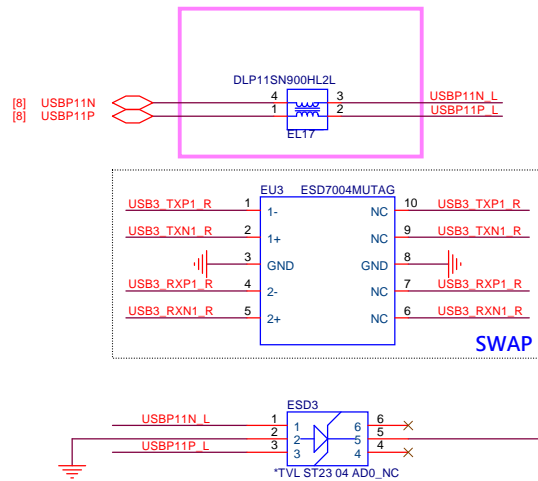
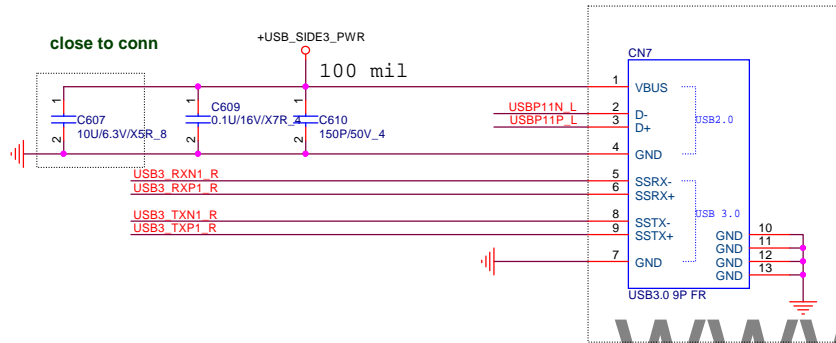
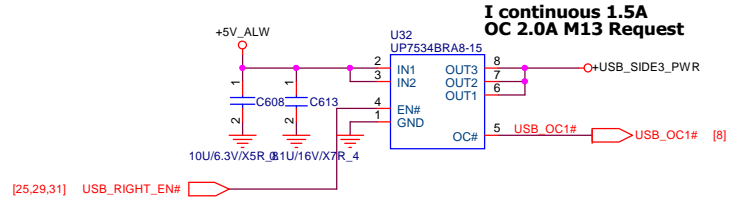
**PROJECT : R07**

Size	Document Number	Rev
		1A
Date:	Monday, June 25, 2012	Sheet 36 of 55

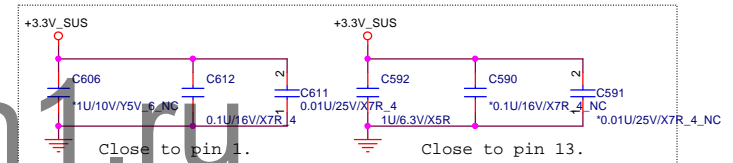
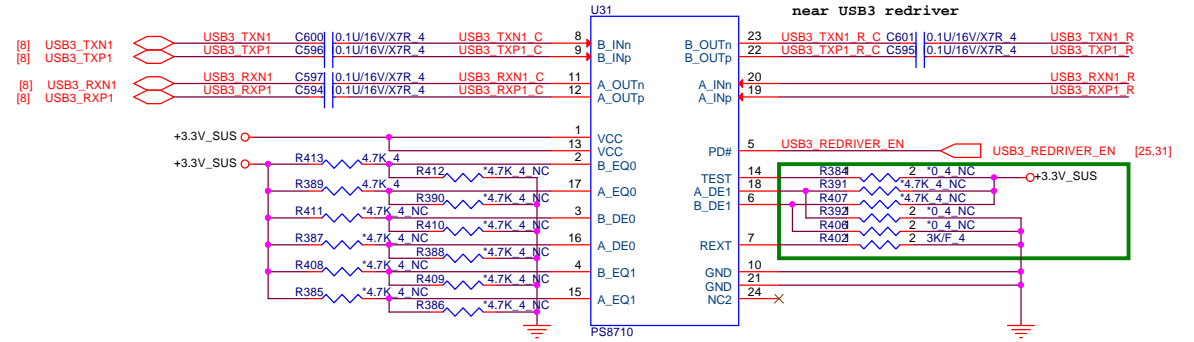
**System Reset Circuit**







Del Colay reserve



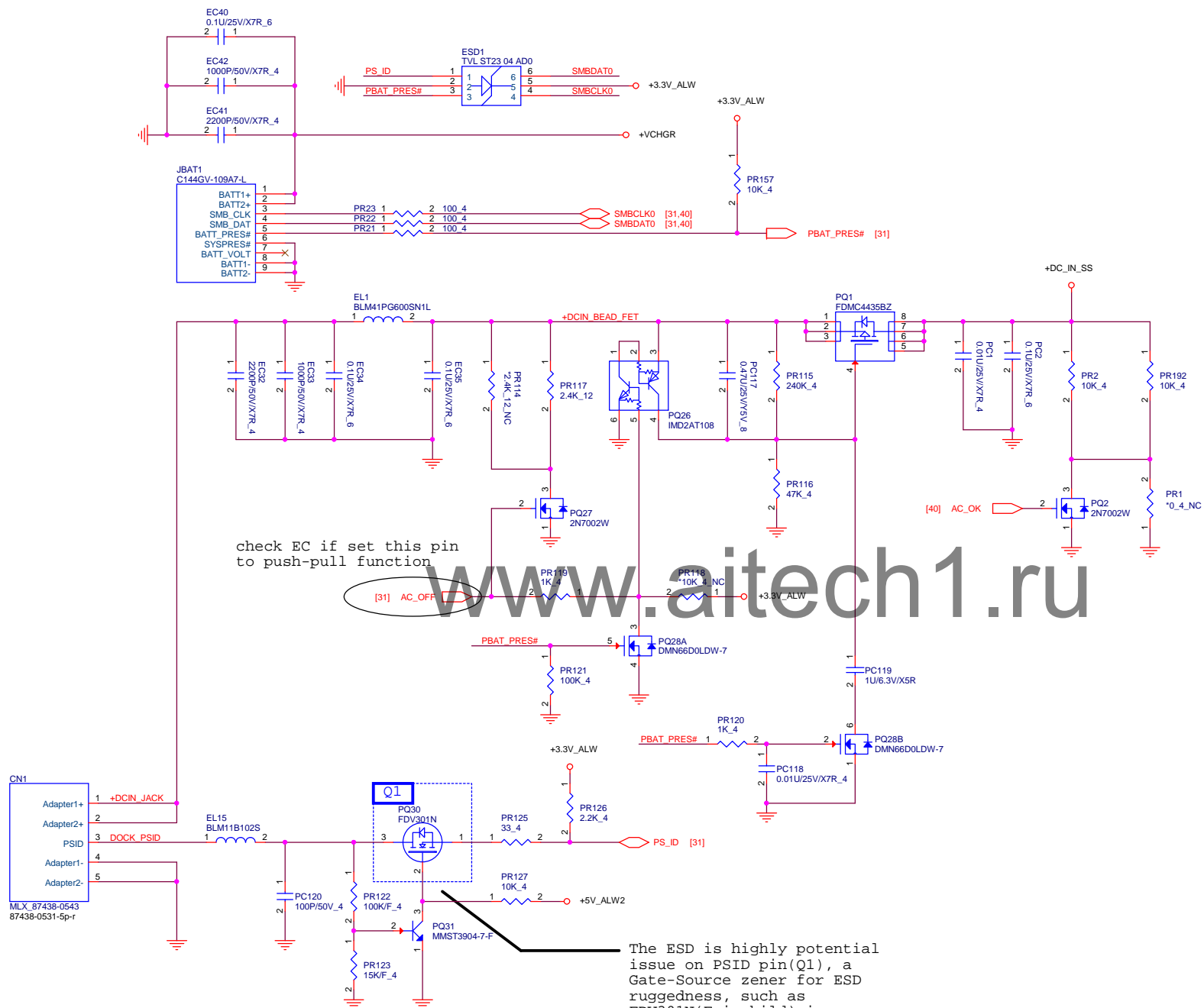
Chip test mode enable.  
3.3V tolerant. Internally pulled down at ~ 150K ohm  
TEST ==  
L: Normal operation (default)  
H: Test mode enable

Programmable output pre-emphasis level setting for channel A  
3.3V tolerant. Internally pulled down at ~ 150K ohm  
[A\_DE1, A\_DE0] ==  
LL: 3.5dB de-emphasis  
LH: No de-emphasis  
HL: 7dB de-emphasis with boost output swing  
HH: 5dB de-emphasis with boost output swing

Equalizer control and program for channel A  
3.3V tolerant. Internally pulled down at ~ 150K ohm  
[A\_EQ1, A\_EQ0] ==  
LL: adaptive EQ enable  
LH: program EQ for channel loss up to 7dB  
HL: program EQ for channel loss up to 14.5dB  
HH: program EQ for channel loss up to 11.5dB

Programmable output pre-emphasis level setting for channel B  
3.3V tolerant. Internally pulled down at ~ 150K ohm  
[B\_DE1, B\_DE0] ==  
LL: 3.5dB de-emphasis  
LH: No de-emphasis  
HL: 7dB de-emphasis with boost output swing  
HH: 5dB de-emphasis with boost output swing

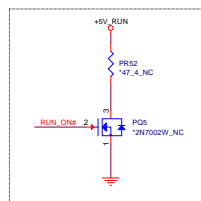
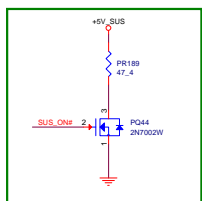
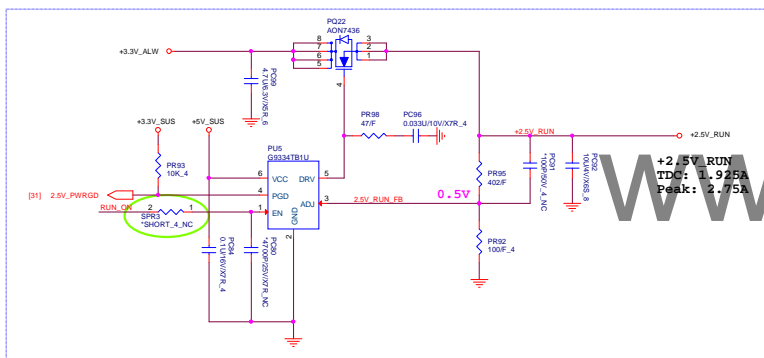
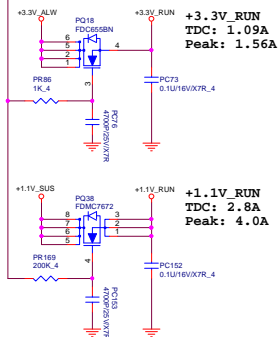
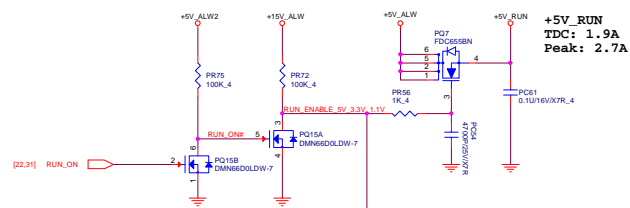
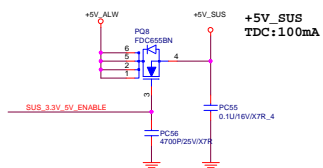
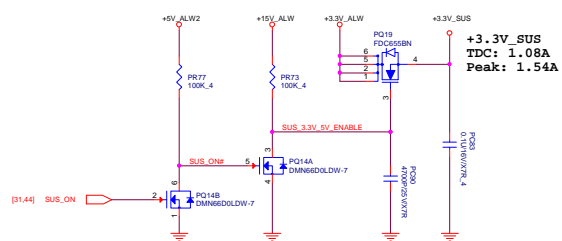
Equalizer control and program for channel B  
3.3V tolerant. Internally pulled down at ~ 150K ohm  
[B\_EQ1, B\_EQ0] ==  
LL: adaptive EQ enable  
LH: program EQ for channel loss up to 7dB  
HL: program EQ for channel loss up to 14.5dB  
HH: program EQ for channel loss up to 11.5dB



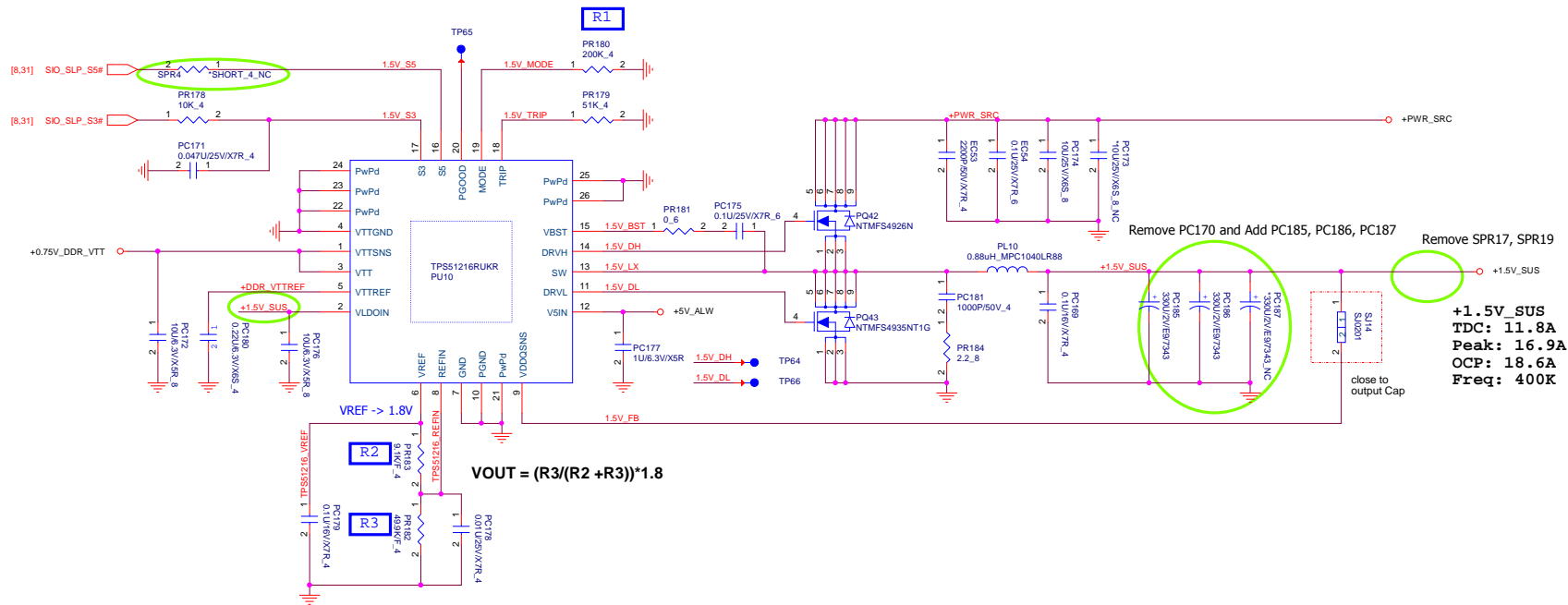
Adapter type	65W	90W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	3.7A	5.6A

Register Address	Register Name
0x12H	ChargeOption()
0x14H	ChargeCurrent()
0x15H	ChargeVoltage()
0x3FH	InputCurrent()
0xFEH	ManufacturerID()
0xFFH	DeviceID()

<default>



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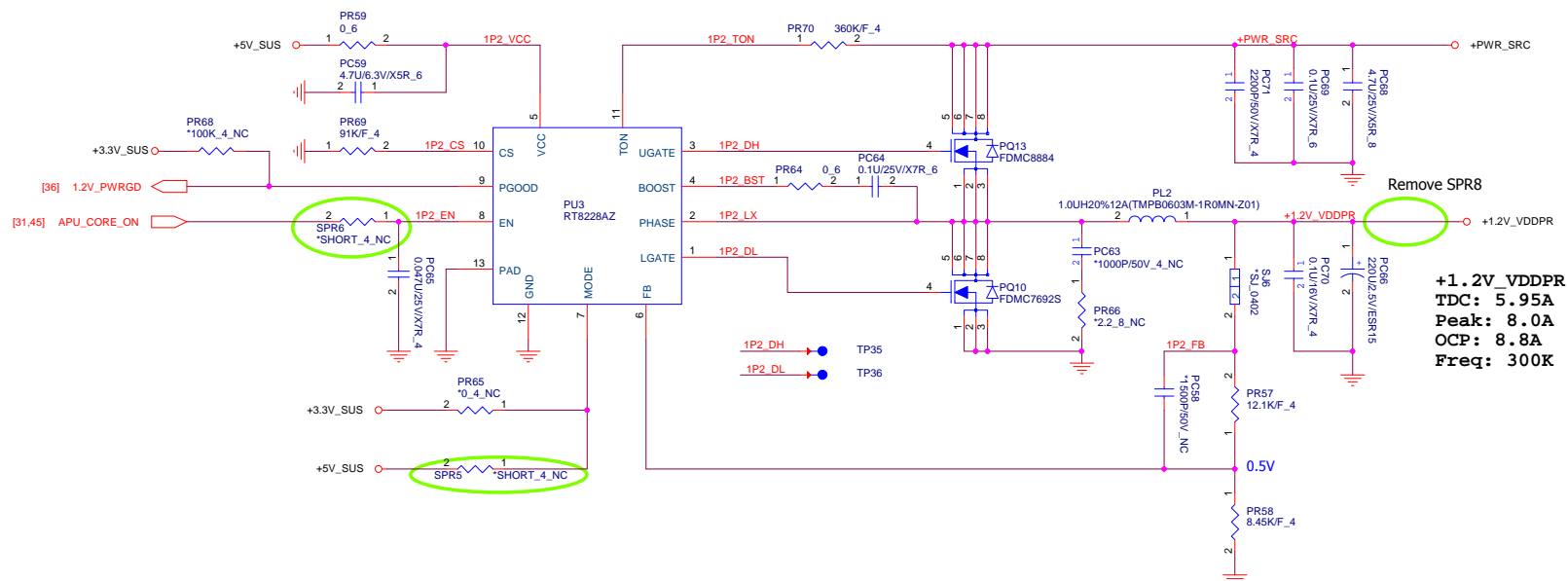
Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)

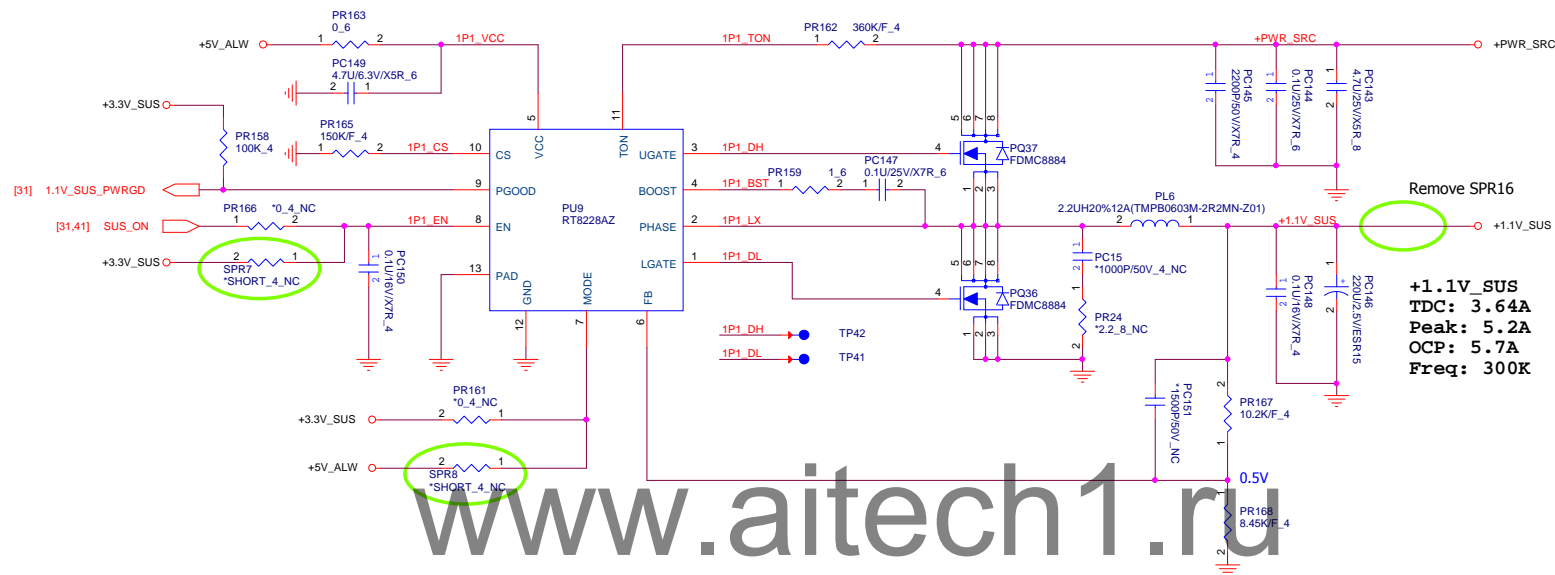
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MODE Selection				
	Resistance between MODE and GND		Frequency	Discharge Mode
R1	200K_4	CS42002JB14	400k Hz	Tracking Discharge
R1	100K_4	CS41002JB20	300k Hz	
R1	68K_4	CS36802JB12	300k Hz	Non-tracking
R1	47K_4	CS34702JB21	400k Hz	Discharge

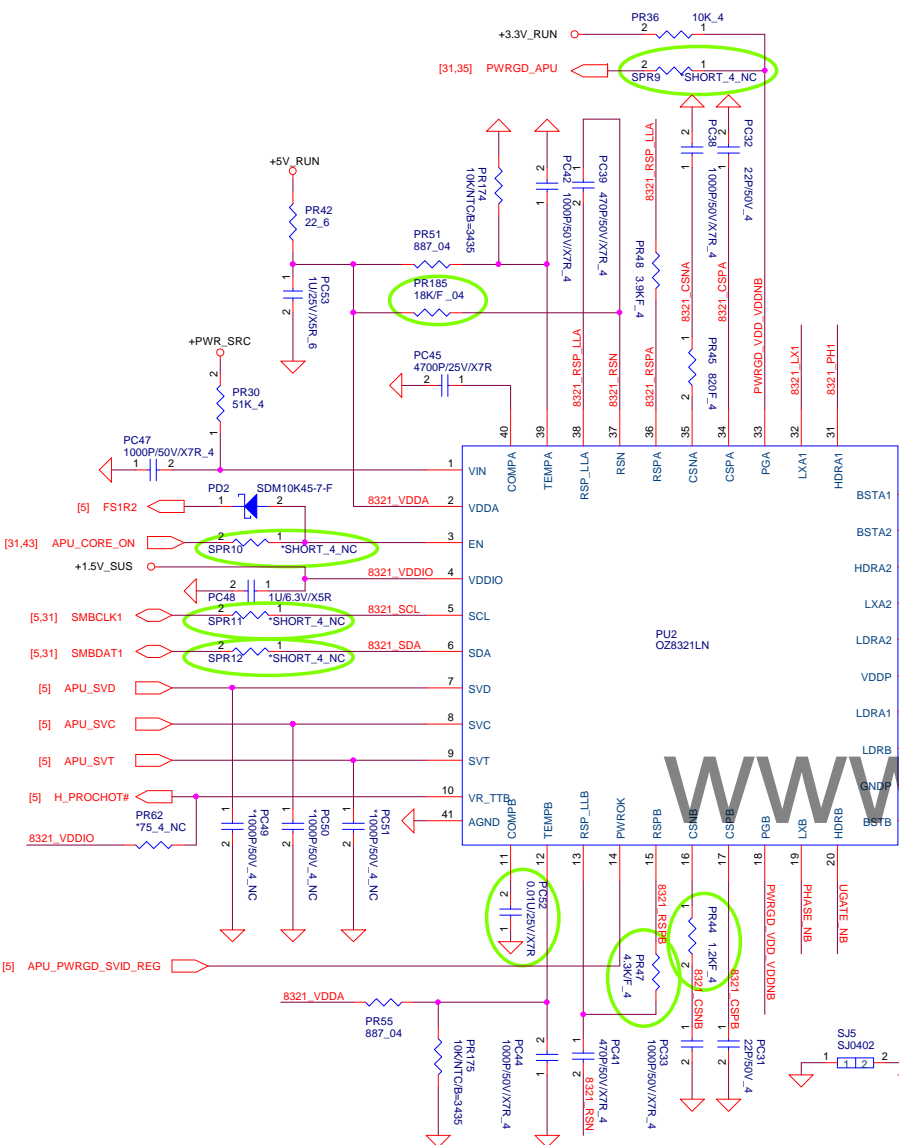
		<b>Quanta Computer Inc.</b> <b>PROJECT : R0AA</b>	
		Size: <b>+1.5V_DDR/0.75V(TPS51216)</b> Date:	Rev: B Sheet 42 of 55



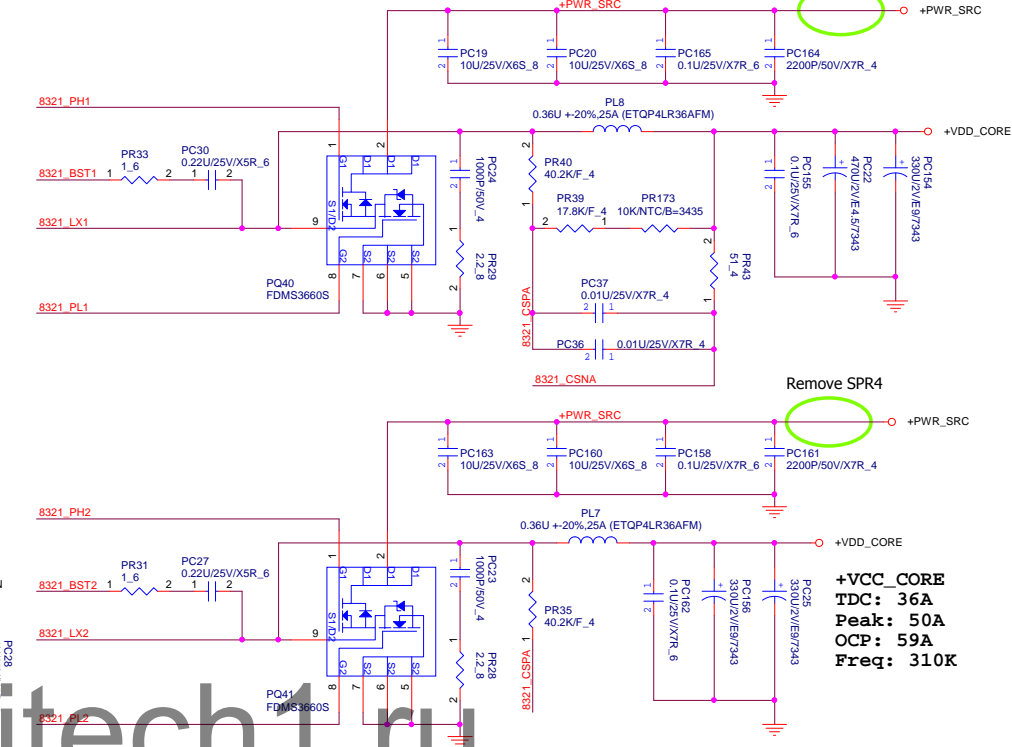
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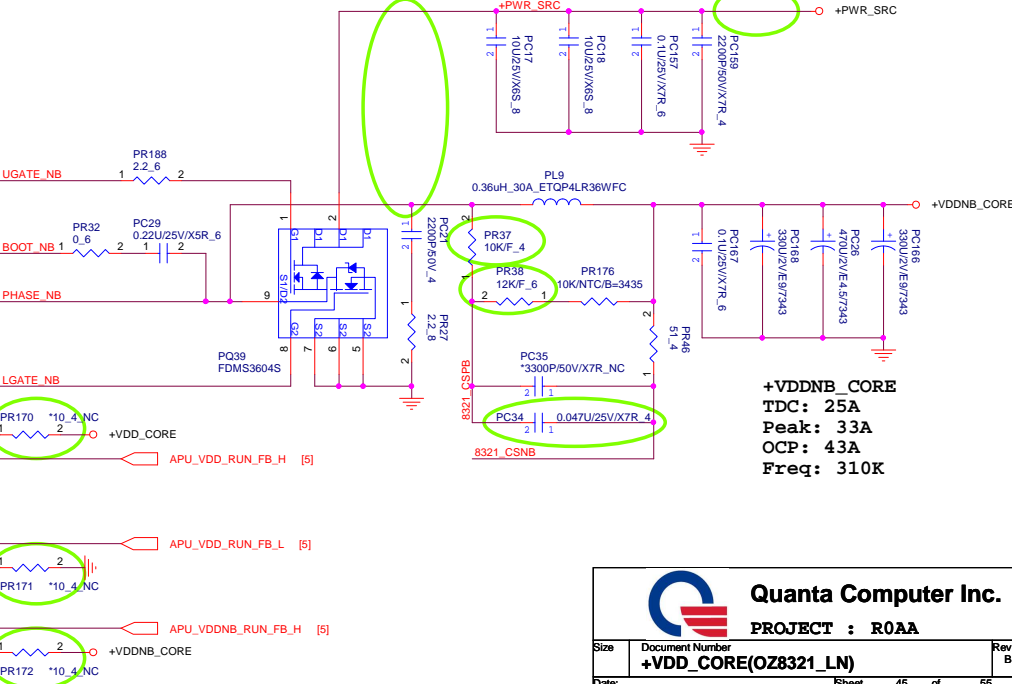




# VDD\_CORE

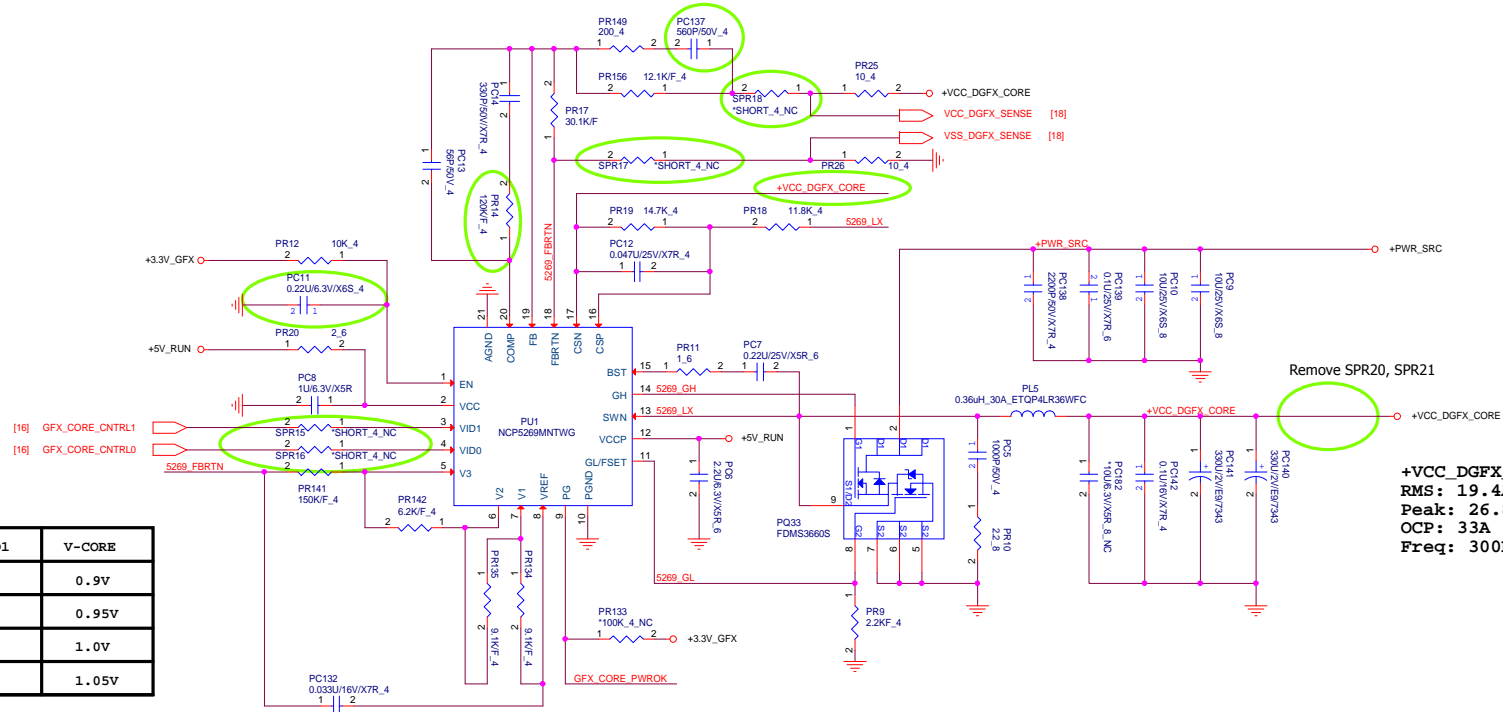


# VDDNB\_CORE

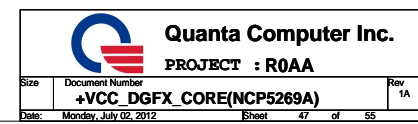


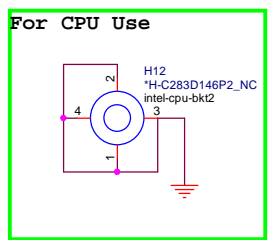
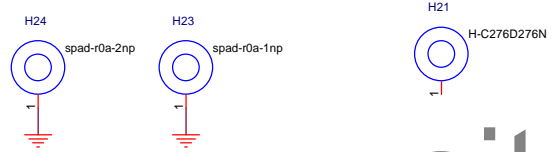
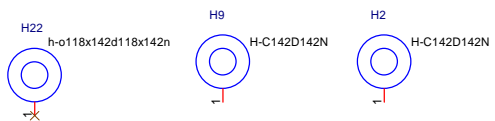
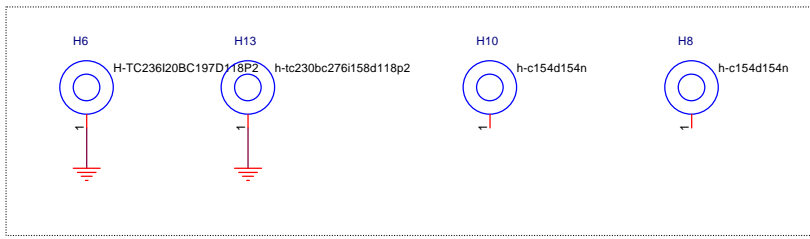
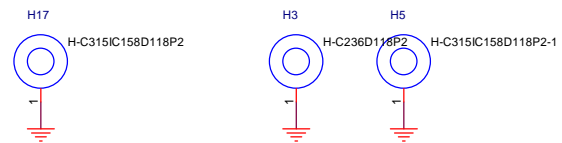
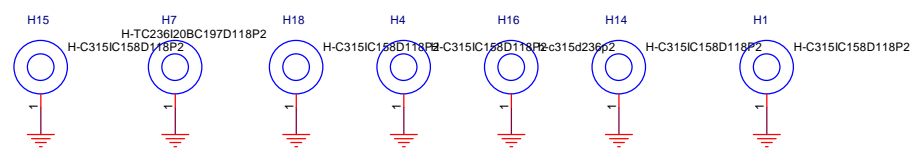
Register Name		Default Value		Address (HEX)		Notes
		Value	Hex	i2C	R/W	
Initial_offset	RailA	0V	00H	A1H	Default	
	RailB	0V	00H	E1H	Default	
IDDSpike	RailA	64A	0FH	A3H	Default	
	RailB	32A	0FH	E3H	Default	
Slew rate	RailA	10mV/us	03H	A4H	Default	
	RailB	10mV/us	03H	E4H	Default	
Special offset	RailA	0V	00H	A8H	Default	
	RailB	0V	00H	E8H	Default	
Temp_max	RailA	100C	01H	A6H	Default	
	RailB	100C	01H	or E6H	Default	
Freq	RailA	3.06usV	12H	A5H	Setting by EC	
	RailB	3.06usV	12H	or E5H	Setting by EC	





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